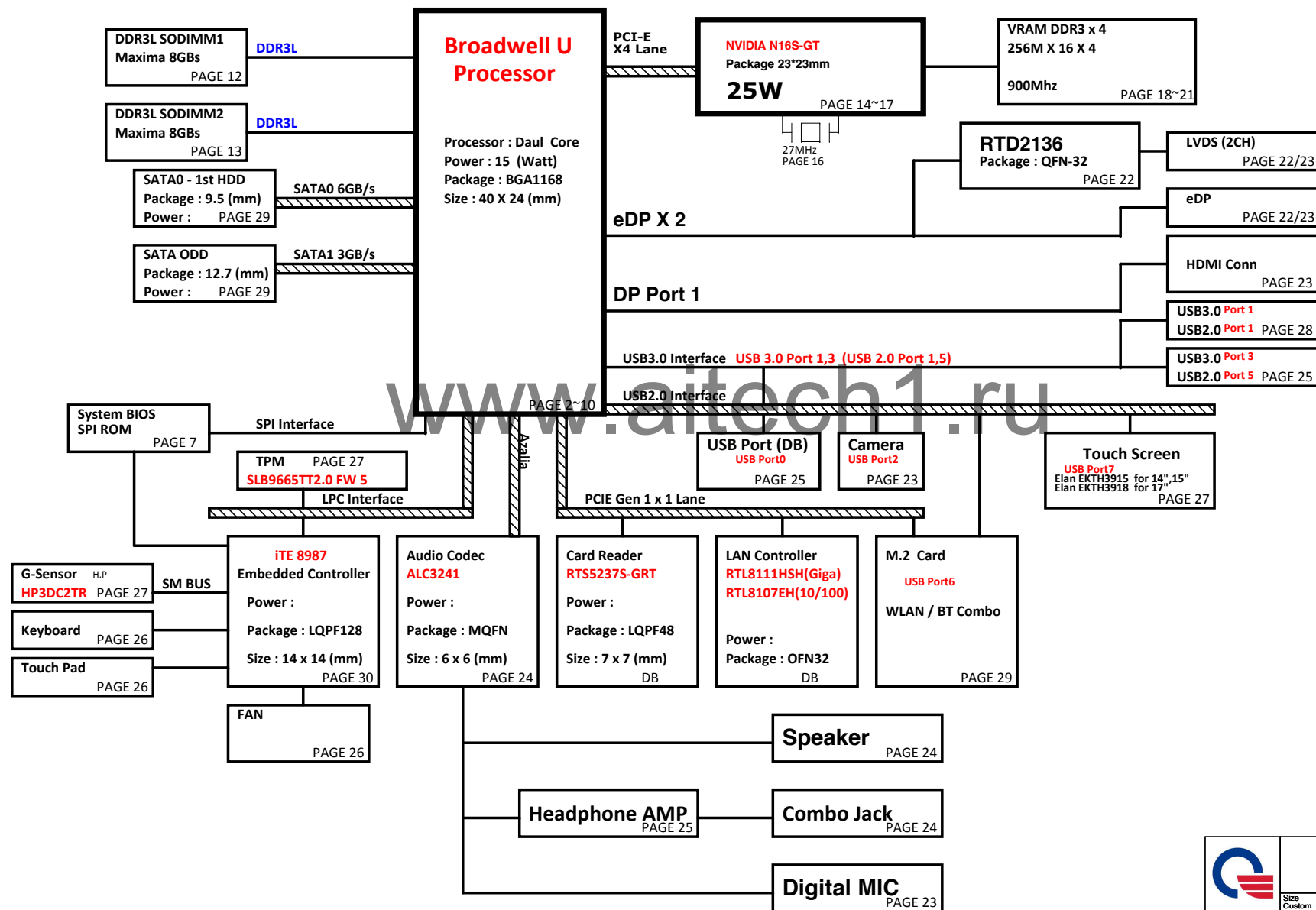


X12 DIS/UMA Single Rank (14" / 15" / 17") Chocolate Intel Crescent Bay ULT Platform Block Diagram

PCB 6L STACK UP

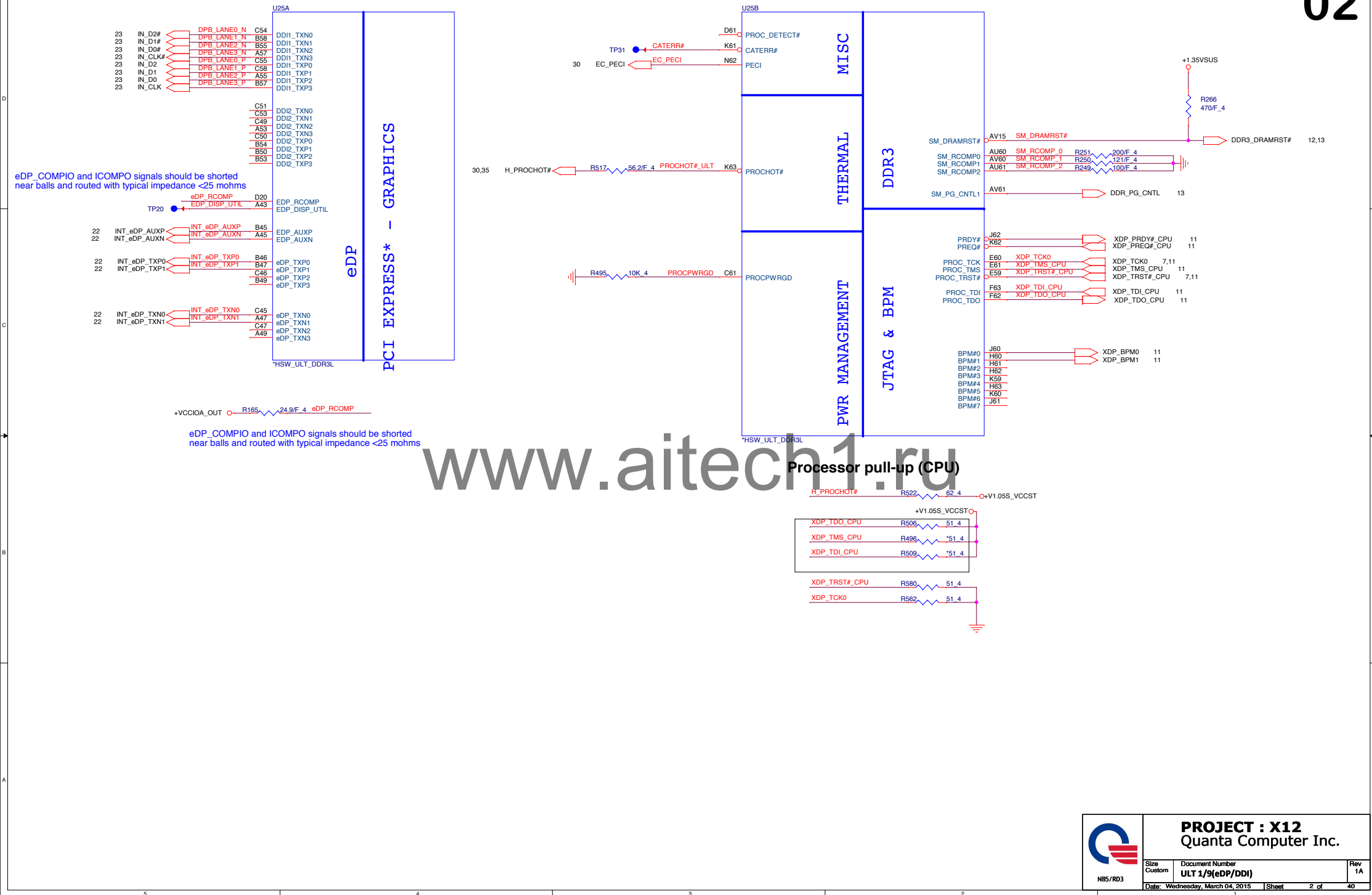
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : GND



PROJECT : X12
Quanta Computer Inc.

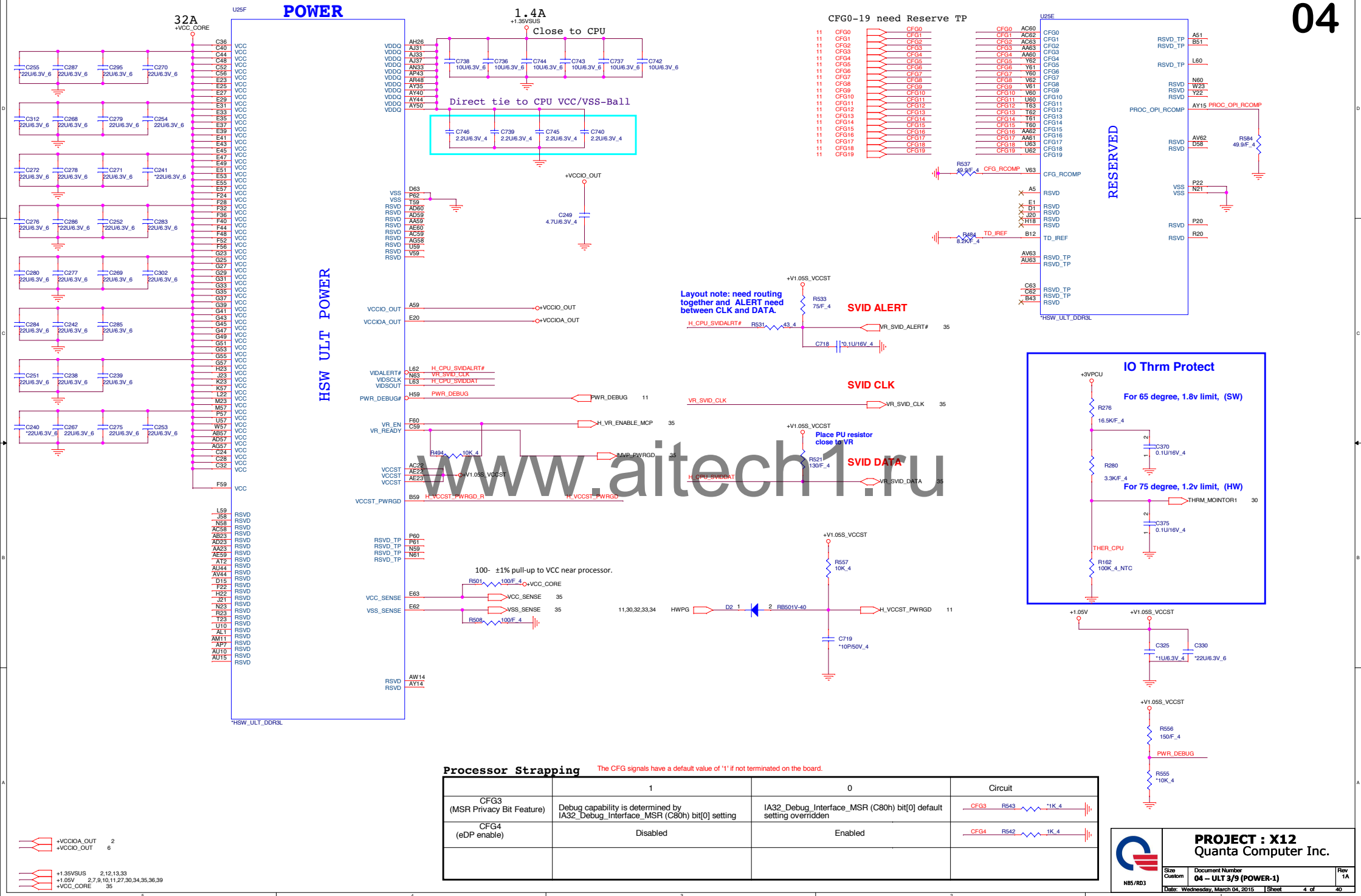
| | | |
|---------------------------------|----------------------------------|-----------|
| Size Custom | Document Number Block Diagram | Rev 1A |
| Date: Wednesday, March 04, 2015 | Sheet | 1 of 40 |

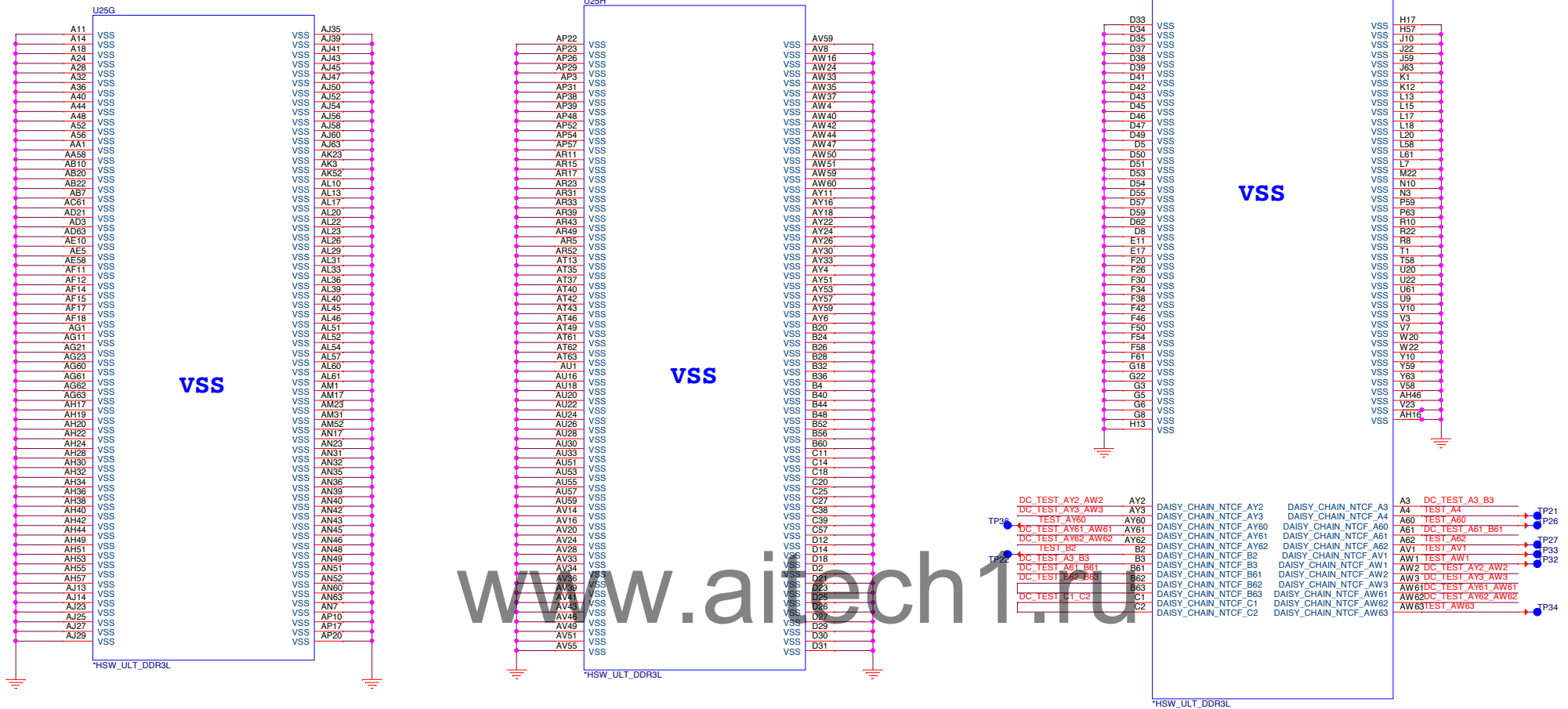
NBS/RD3



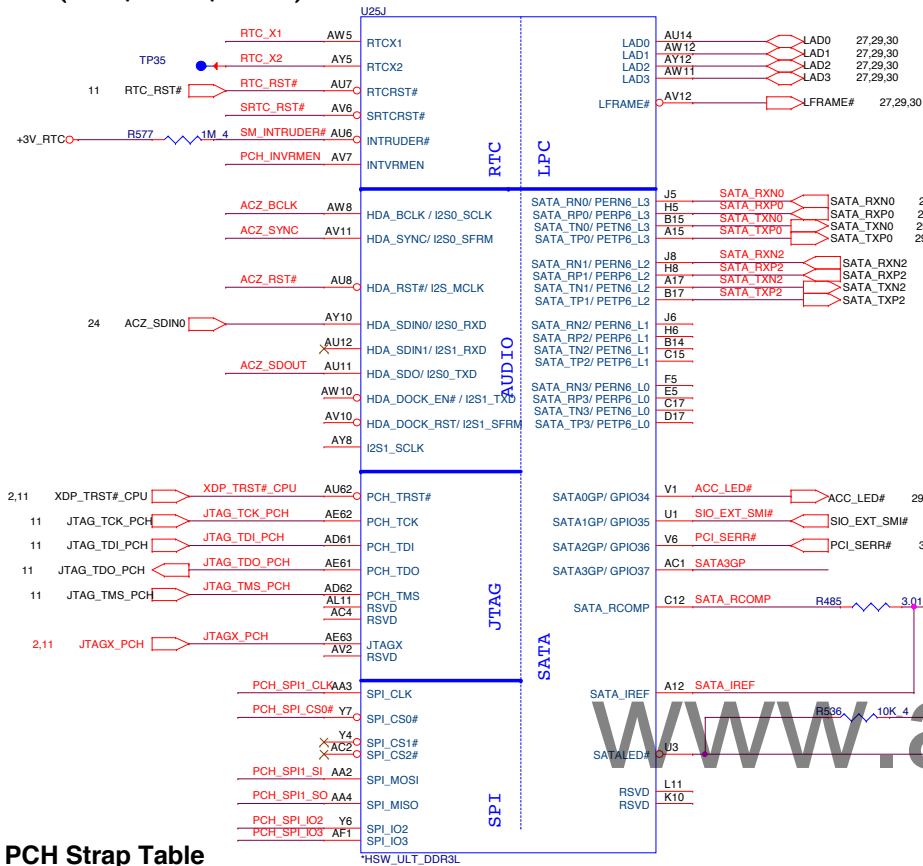
A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B has a right-pointing arrow on its left side.





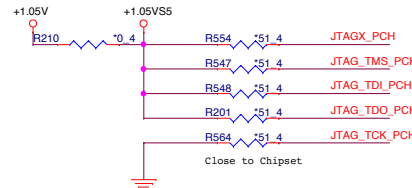


Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)







HDD (SATA3 6.0Gb/s)

ODD (SATA2 3.0Gb/s)

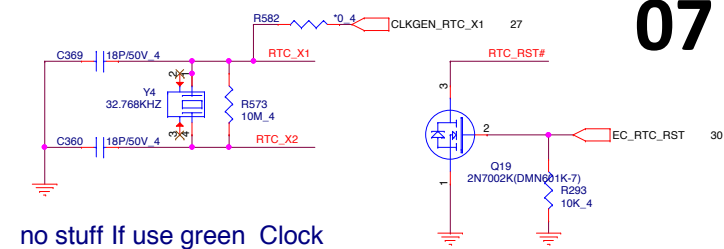


DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

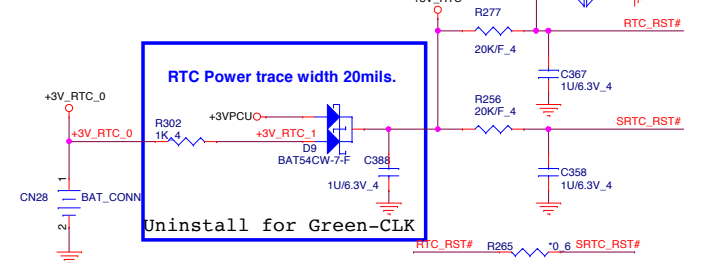
PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | Circuit | | | | | | |
|--------------------|--|---------|--|---|---------------|---|-----|---|--------------|--|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode | | | | | | | |
| SDIO_D0 /GPIO66 | Top-Block Swap | PWROK | 0 = "top-block swap" mode 1 = Default (weak pull-up 20K) | | | | | | | |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up |  | | | | | | |
| HDA_SDO /I2S0_TXD | Flash Descriptor Security Only for Interposer | PWROK | 0 = Default (weak pull-down 20K) 1 = Can be Overriden |  | | | | | | |
| GSPI0_MOSI /GPIO86 | Boot BIOS Selection | PWROK | <table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></tbody></table> | GNT0# | Boot Location | 1 | LPC | 0 | SPI(Default) | |
| GNT0# | Boot Location | | | | | | | | | |
| 1 | LPC | | | | | | | | | |
| 0 | SPI(Default) | | | | | | | | | |
| GPIO15 | TLS Confidentiality | PWROK | 0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality | | | | | | | |
| DSWVRMEN | Deep Sx Well On-Die Voltage Regulator Enable | ALWAYS | Should be always pull-up |  | | | | | | |
| | | | |  | | | | | | |

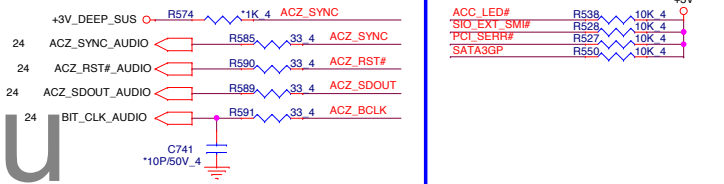
RTC Clock 32.768KHz



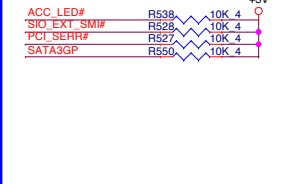
RTC Circuitry(RTC)



HDA Bus(CLG)



GPIO Pull UP

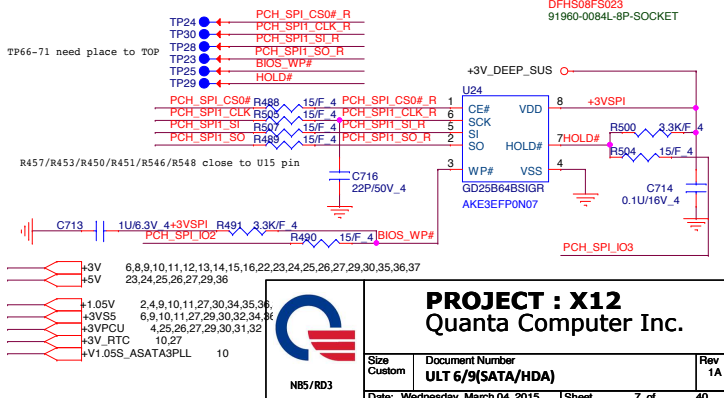


| Vender | Size | P/N |
|------------|------|-------------------------------|
| EON | 8MB | AKE3EZN0Q01 (EN25QH64-104HIP) |
| Winbond | 8MB | AKE3EFP0N07 (W25Q64FVSSIQ) |
| GigaDevice | 8MB | AKE3EGN0Q01 (GD25B64BSIGR) |
| Socket | | DFHS08FS023 |

4M SPI ROM Socket

U23&U24 footprint 要重疊

PCH SPI ROM(CLG)

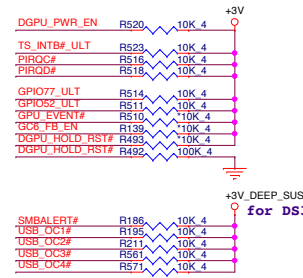


PROJECT : X12
Quanta Computer Inc.

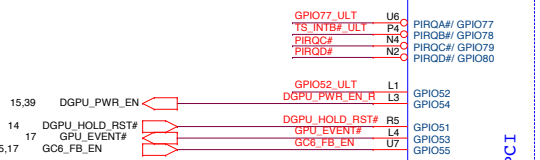
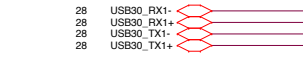
| | | |
|---------------------------------|---|---------------|
| Size Custom | Document Number ULT 6/9(SATA/HDA) | Rev 1A |
| Date: Wednesday, March 04, 2015 | | Sheet 7 of 40 |

Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

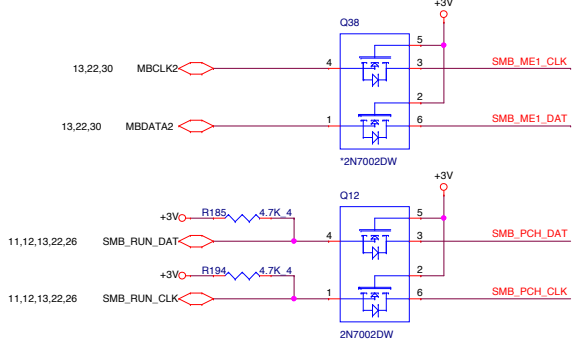
PCI/USB OC# Pull-up (CLG)



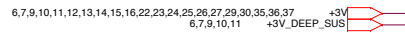
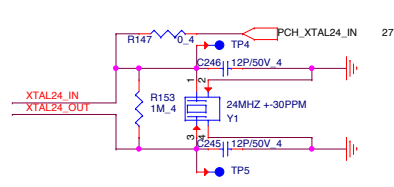
USB3.0 M/B



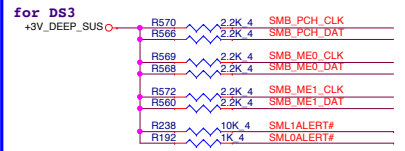
SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)

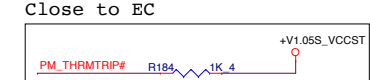
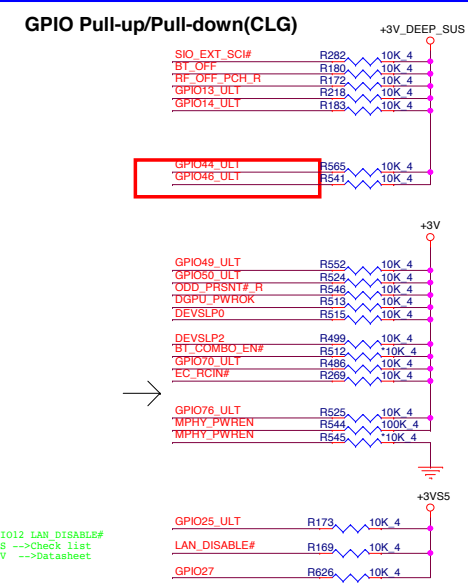
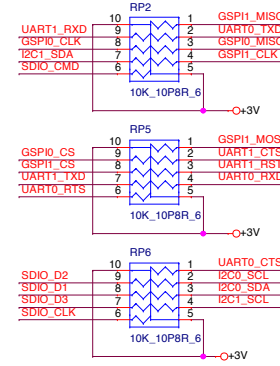
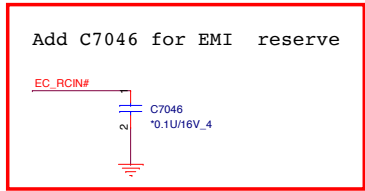
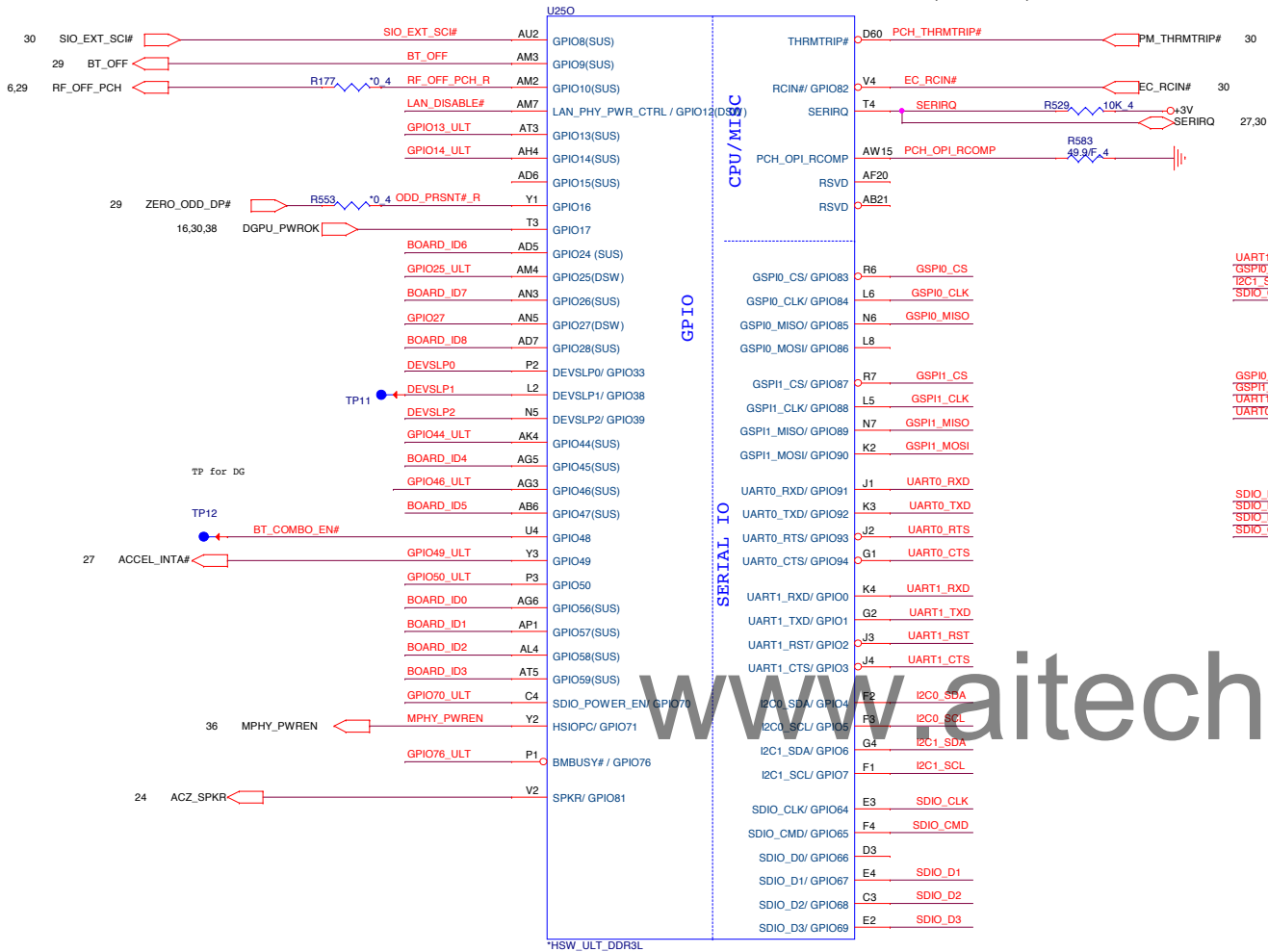


PROJECT : X12
Quanta Computer Inc.

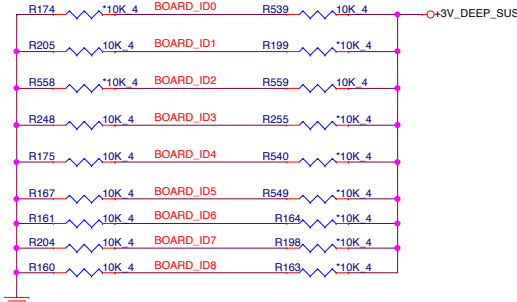
| | | |
|---------------------------------|--|-----------|
| Size Custom | Document Number ULT 7/9 (PCIE/USB/CLK) | Rev 1A |
| Date: Wednesday, March 04, 2015 | Sheet | 8 of 40 |

Lynx Point-LP Platform Controller Hub
(HDA,JTAG,SATA) Haswell (GPIO)

09



| Model | BOARD_ID[8:7] | BOARD_ID[6:5] | Board ID [4:3] | BOARD_ID[2:1] | BOARD_ID0 |
|------------|---------------------------|---------------------------|---|----------------------------|--------------------|
| Definition | Reserve (Default = 00) | Reserve (Default = 00) | 00 Single Rank (X12) 01 DUAL Rank (X12) 10 Meso-AMD (X11) 11 Reserve | 00 14" 01 15" 10 17" | 0 : UMA 1 : DIS |

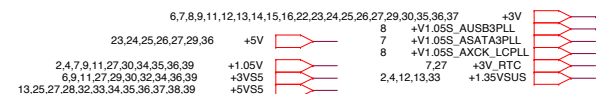
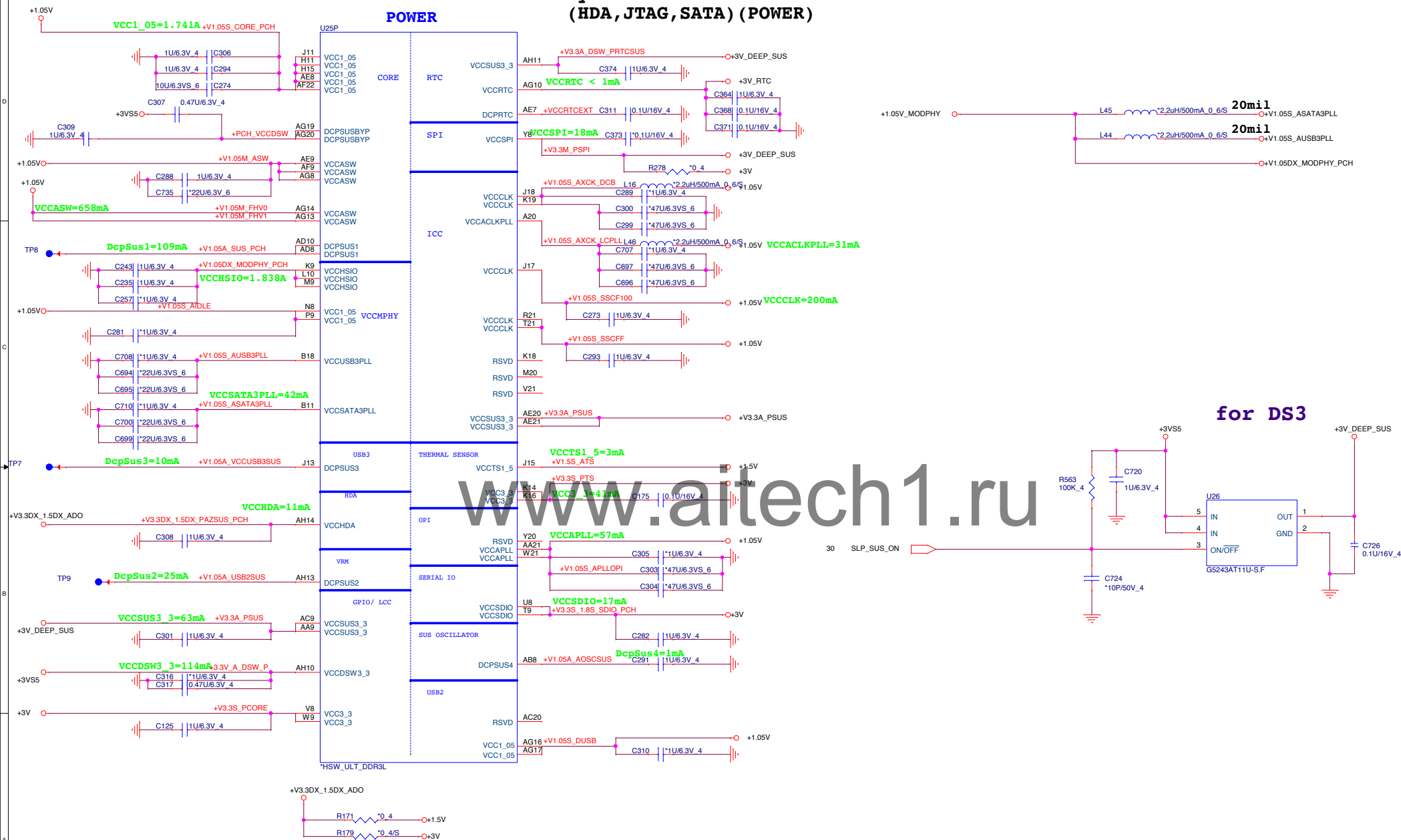


6,7,8,10,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37
6,10,11,27,29,30,32,34,36,39

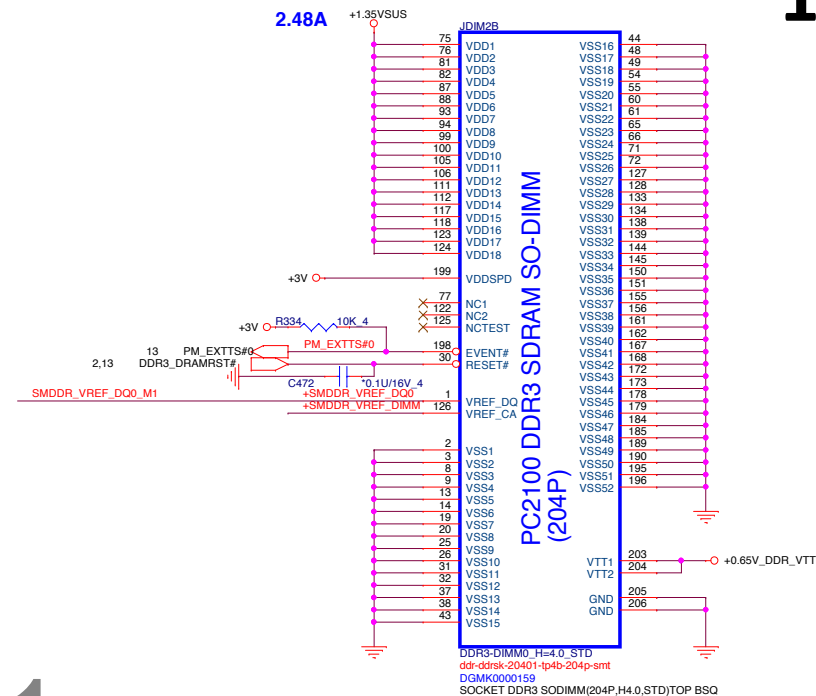
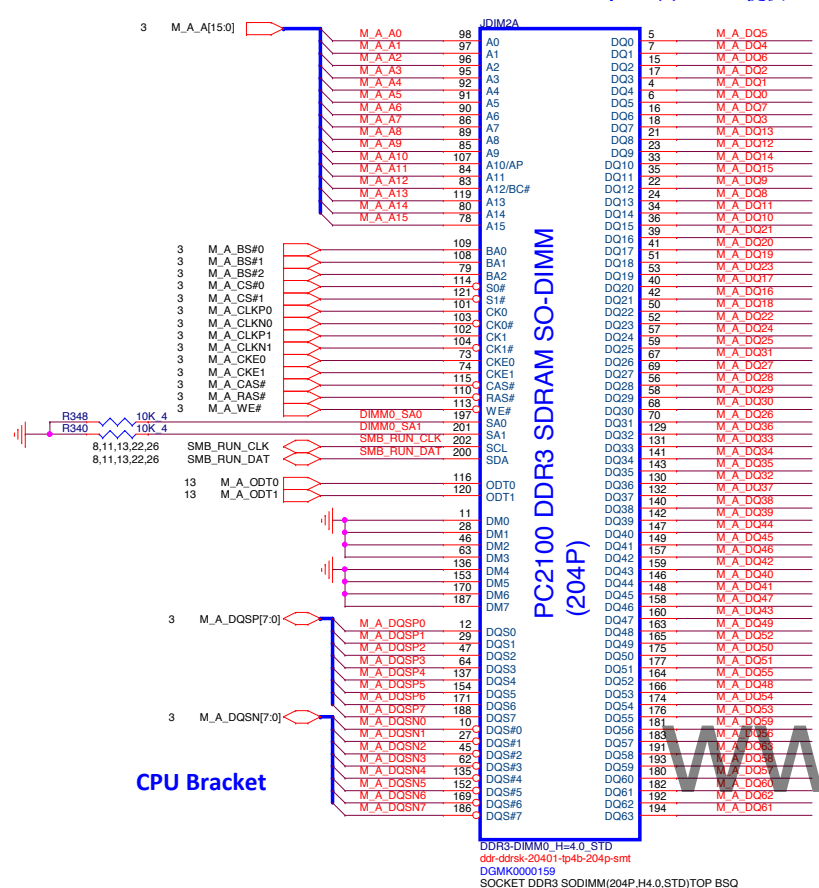
+3V
+3VSS

PROJECT : X12
Quanta Computer Inc.

| | | |
|---------------------------------|---|---------------|
| Size Custom | Document Number ULT 8/9 (GPIO/MISC) | Rev 1A |
| Date: Wednesday, March 04, 2015 | | Sheet 9 of 40 |

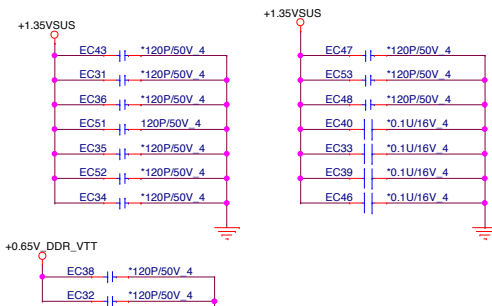






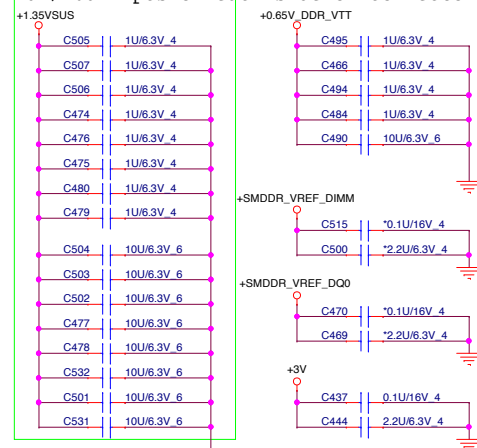
174 M. A. DO54
176 M. A. DO53
181 M. A. DO59
183 M. A. DO56
191 M. A. DO63
193 M. A. DO58
180 M. A. DO57
182 M. A. DO60

For EMI RESERVE

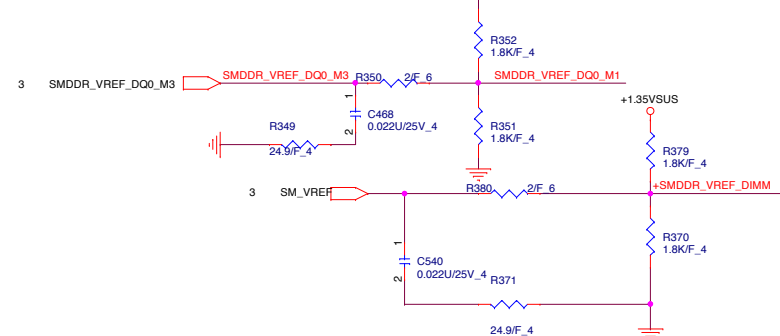


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



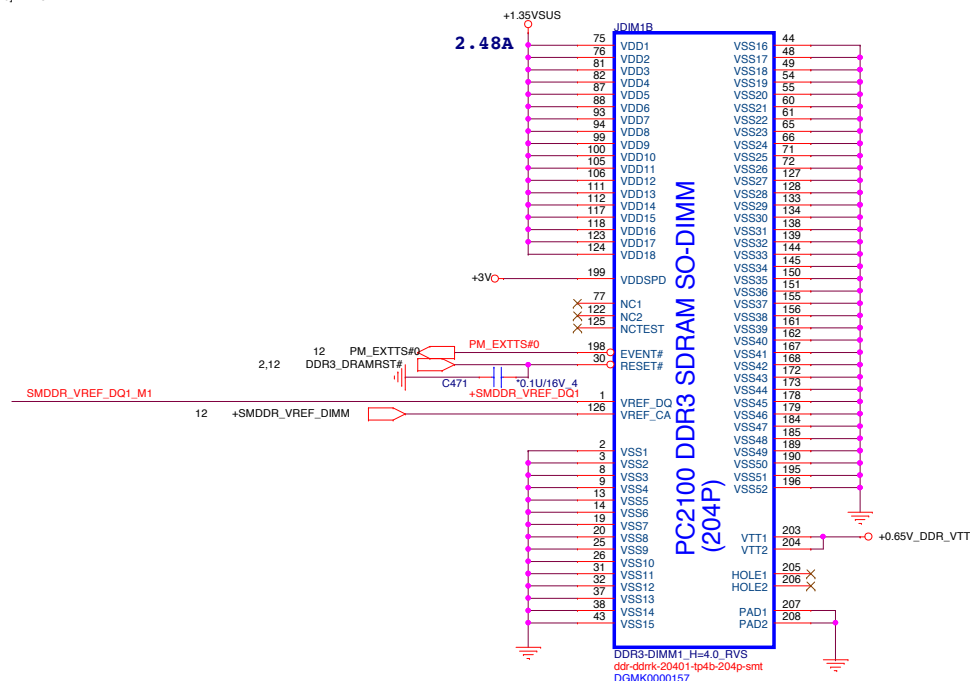
VREF DQ0 M1 Solution



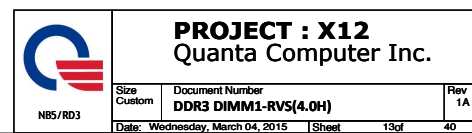
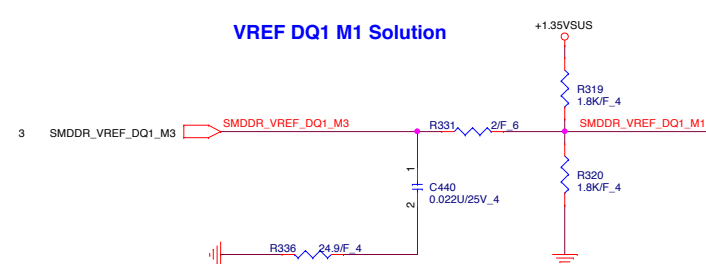
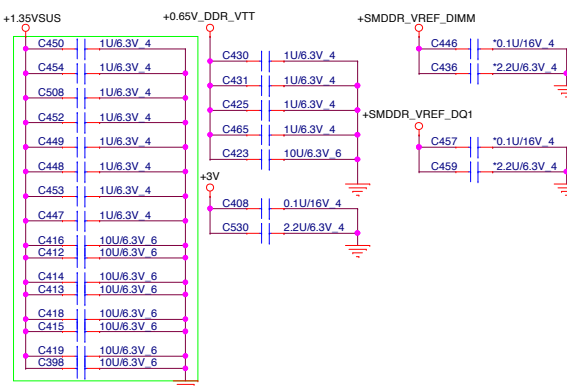
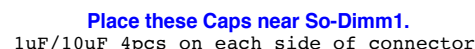
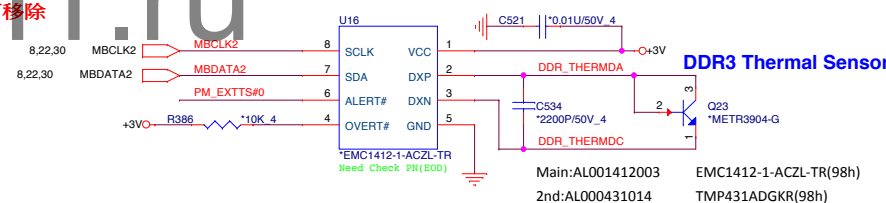
PROJECT : X12
Quanta Computer Inc.

| | | |
|---------------------------------|--|-----------|
| Size Custom | Document Number DDR3 DIMM0-STD(4.0H) | Rev 1. |
| Date: Wednesday, March 04, 2015 | Sheet | 12 of 40 |

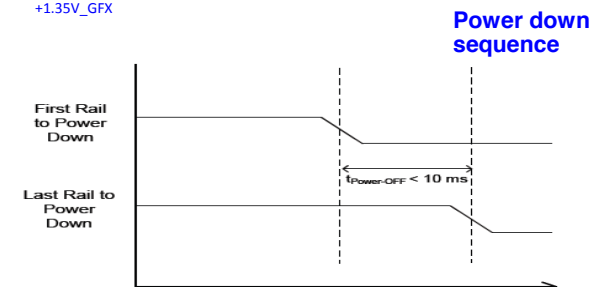
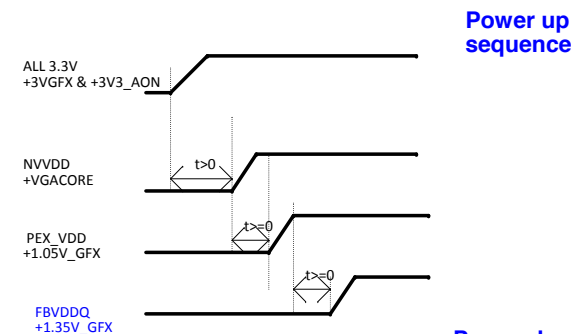
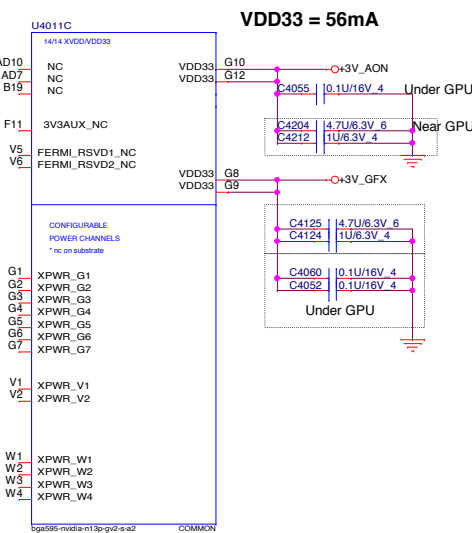
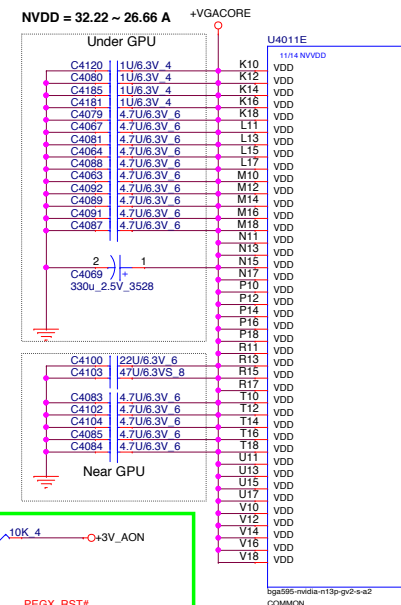
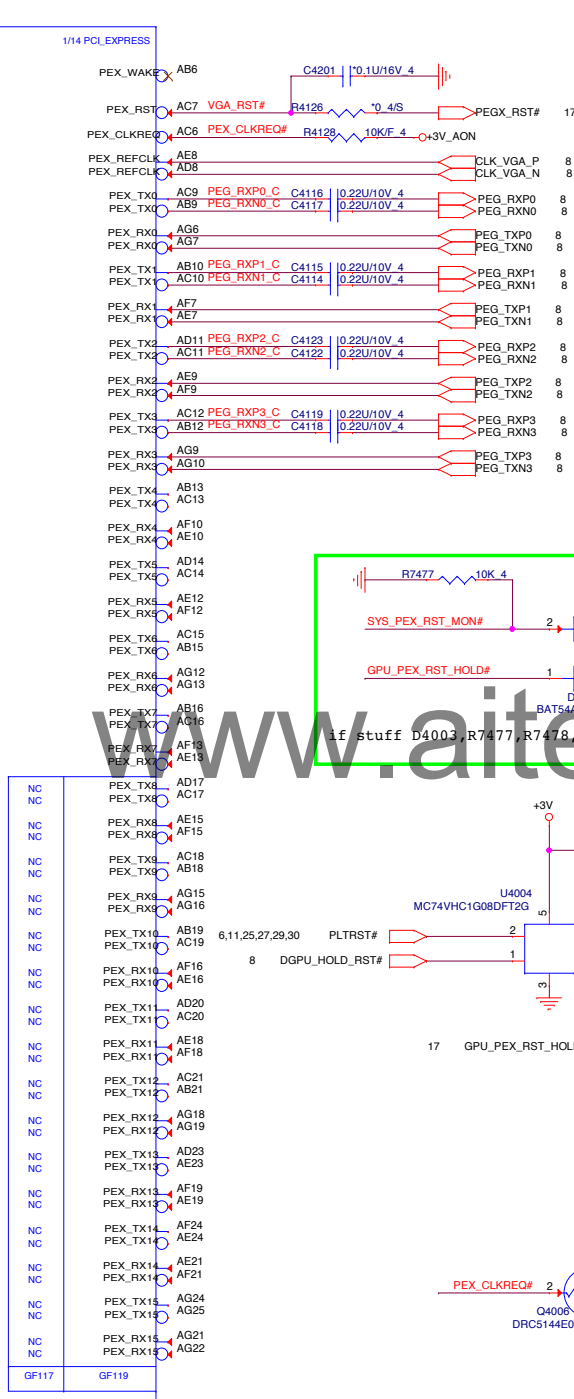
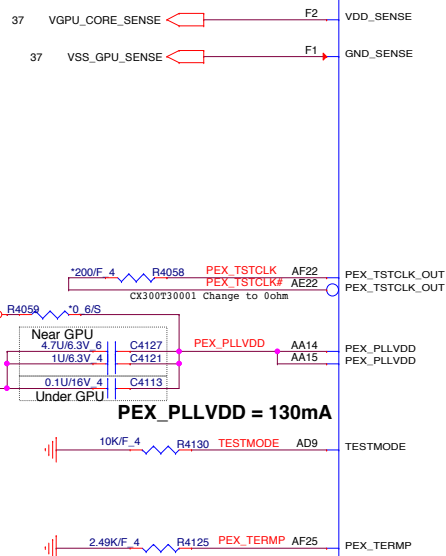
M B DQ[63:0]

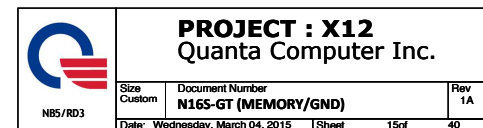


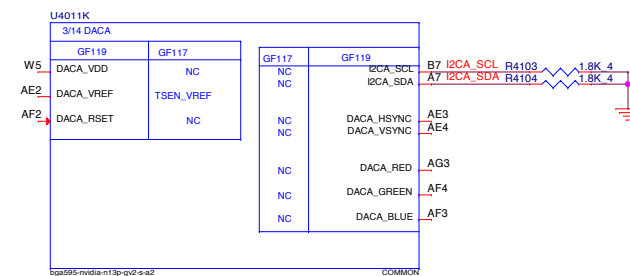
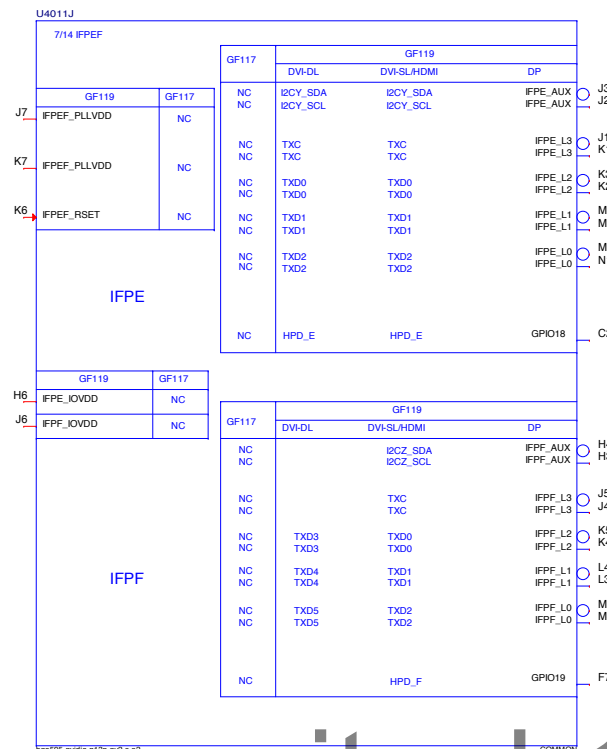
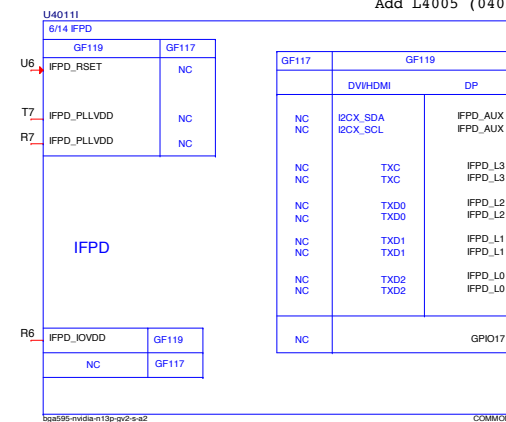
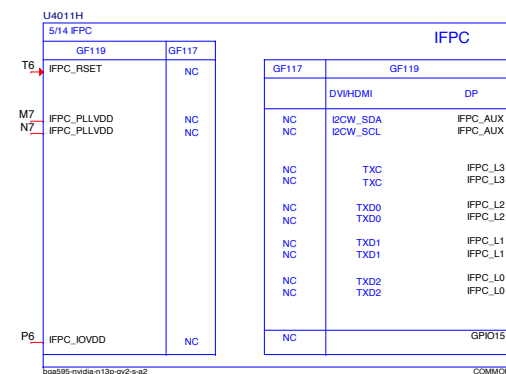
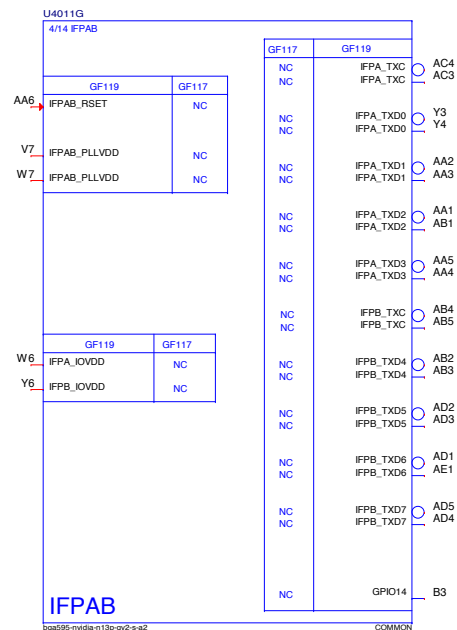
| | | |
|------|-----|----------|
| DQ52 | 166 | M B DQ55 |
| DQ53 | 174 | M B DQ50 |
| DQ54 | 176 | M B DQ53 |
| DQ55 | 181 | M B DQ63 |
| DQ56 | 183 | M B DQ82 |
| DQ57 | 191 | M B DQ59 |
| DQ58 | 193 | M B DQ57 |
| DQ59 | 180 | M B DQ56 |
| DQ60 | | |



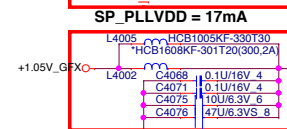
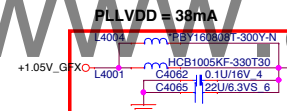
The diagram illustrates the power supply network for the Near GPU. A +3V_AON input is connected to a network of capacitors (C4061, C4172, C4174) and inductors. The network is connected to the AA8, AA9, and AB8 pins of the GPU. The AA8 and AA9 pins are connected to PEX_PLL_HVDD, and the AB8 pin is connected to PEX_SVDD_3V3.



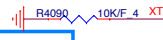




www.aitech1.ru

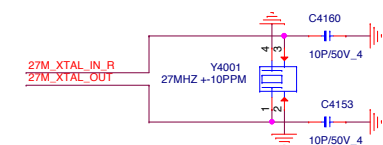
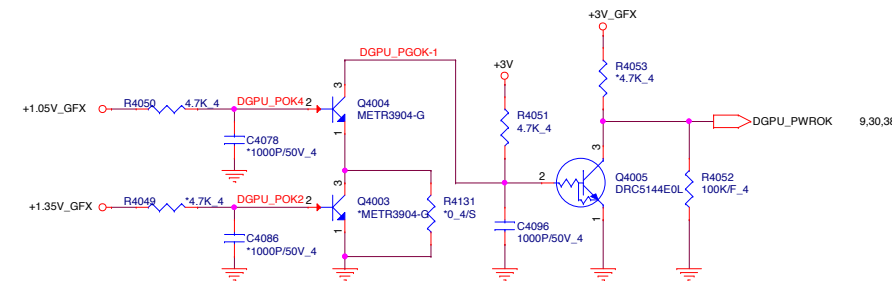


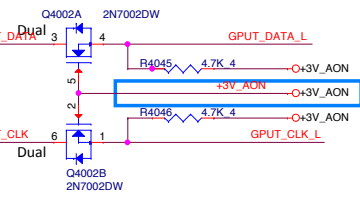
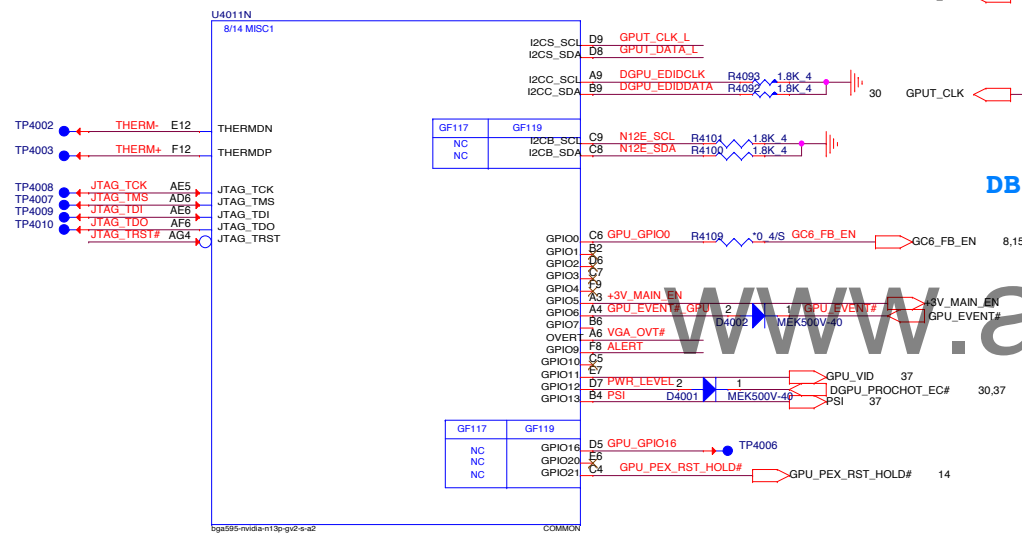
VID_PLLVD = 41mA



DB-->SI change 10/25

Use G-CLK



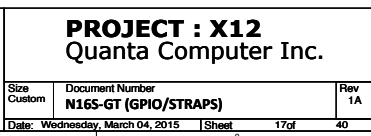


| Resistor Values | Pull-Up to 3V3_MAIN | Pull-Down to GND |
|-----------------|---------------------|------------------|
| 4.99 kΩ | 1000 | 0000 |
| 10.0 kΩ | 1001 | 0001 |
| 15.0 kΩ | 1010 | 0010 |
| 20.0 kΩ | 1011 | 0011 |
| 24.9 kΩ | 1100 | 0100 |
| 30.1 kΩ | 1101 | 0101 |
| 34.8 kΩ | 1110 | 0110 |
| 45.3 kΩ | 1111 | 0111 |

tech1.ru

| VRAM Configuration Table | | ROM | SI | S | F | | |
|--------------------------|----------------------------------|---------|----------------------|-----------|-------------|-------------|--|
| RAMCFG [3:0] | DESCRIPTION | Vendor | Vendor P/N | Strapping | TOP B/S | QBC | |
| 0000 | DDR3L 256Mx16, 64bit, 4Gb,900MHz | HYNIX | H5TC4G63CFR-N0C | 0x2 | AKD5PZDTW01 | AKD5PZDTW02 | |
| 0010 | DDR3L 256Mx16, 64bit, 4Gb,900MHz | Micron | MT41J256M16BA-093G:E | 0x4 | AKD5PZSTL00 | AKD5PZSTL01 | |
| 0100 | DDR3L 256Mx16, 64bit, 4Gb,900MHz | SAMSUNG | K4W4G1646E-BC1A | 0x1 | AKD5PGDT500 | AKD5PGDT501 | |

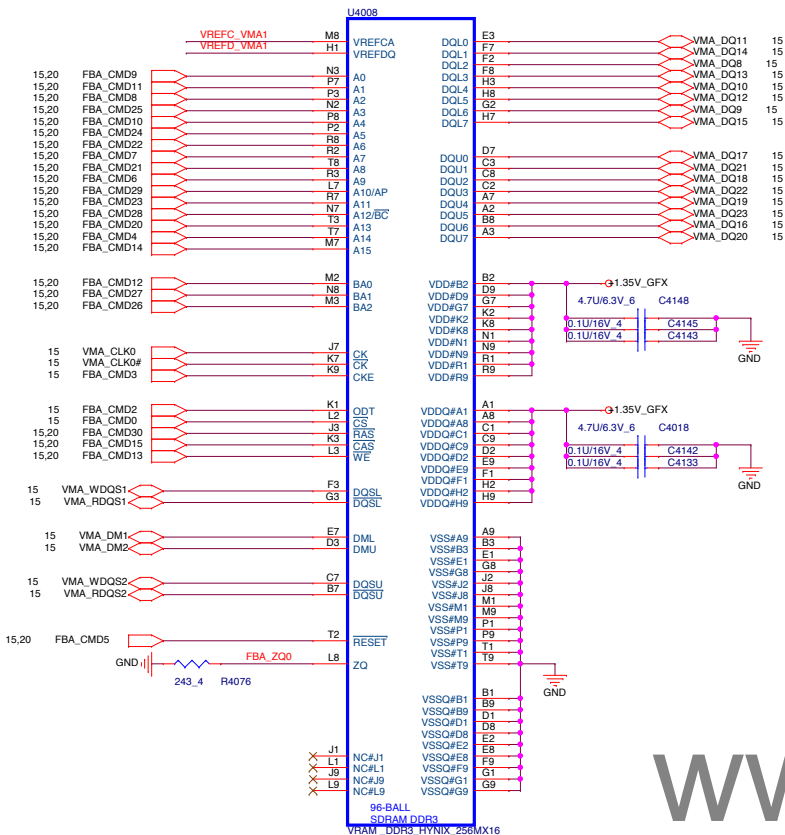
| GPIO | I/O | PIN | USAGE |
|------|-----|------------------|--|
| 0 | IN | FB_CLAMP_MON | FB Clamp monitor |
| 1 | OUT | MEM_VDD_CTL | Memory VDD VID |
| 2 | OUT | LCD_BL_PWM | Panel Backlight PWM |
| 3 | OUT | LCD_VCC | PANEL POWER ENABLE |
| 4 | OUT | LCD_BLEN | PANEL BACKLIGHT ENABLE |
| 5 | OUT | Reserved | -- |
| 6 | OUT | FB_CLAMP_TGL_REQ | Active low FB Clamp toggle request |
| 7 | OUT | 3D_VISION | 3D VISION LEFT/RIGHT signal |
| 8 | I/O | OVERT | ACTIVE LOW THERMAL OVER TEMP |
| 9 | I/O | ALERT | ACTIVE LOW THERMAL ALERT |
| 10 | OUT | MEM_VREF_CTL | MEMORY_VREF CONTROL |
| 11 | OUT | PWR_VID | GPU_CORE_VDD PWM Control signal |
| 12 | IN | PWR_LEVEL | AC Power detect or power supply overdraw input |
| 13 | OUT | PSI | Phase Shedding |



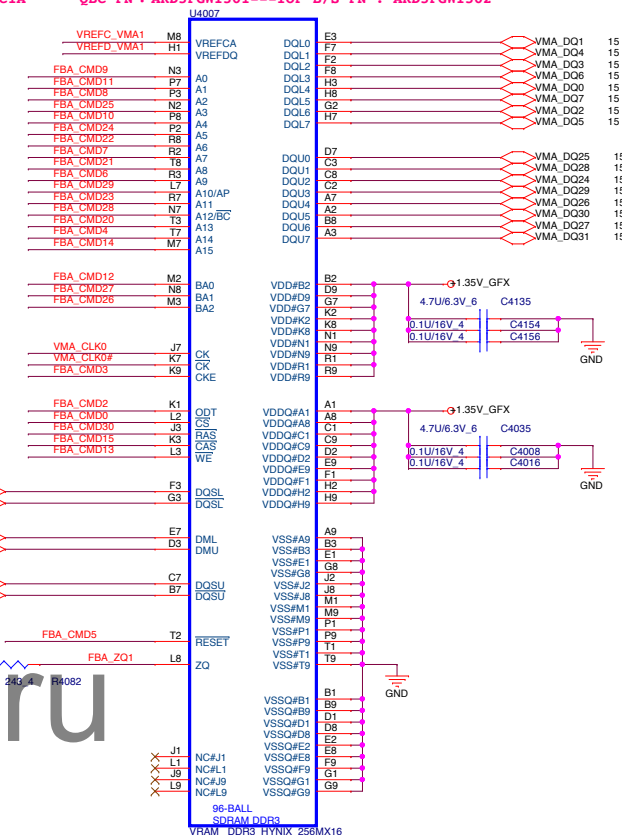
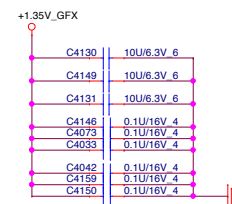
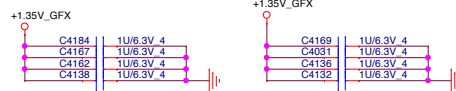
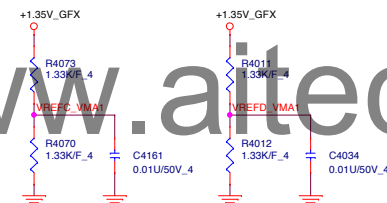
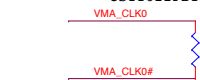
Rank0

HYU 256Mx16, H5TC4G63APR-11C
 MTC 256Mx16, MT411256M16BA-093G:E
 SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGTW08---TOP B/S PN : AKD5PGTW07
 QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 QBC PN : AKD5PGTW501---TOP B/S PN : AKD5PGTW502



162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
 CS11622FB15 RES CHIP 162 1/16W +-1%(0402)




www.aitech1.ru



PROJECT : X12
 Quanta Computer Inc.

Size Custom Document Number DDR3L - RANK0 Rev 1A
 Date: Wednesday, March 04, 2015 1 Sheet 18 of 40

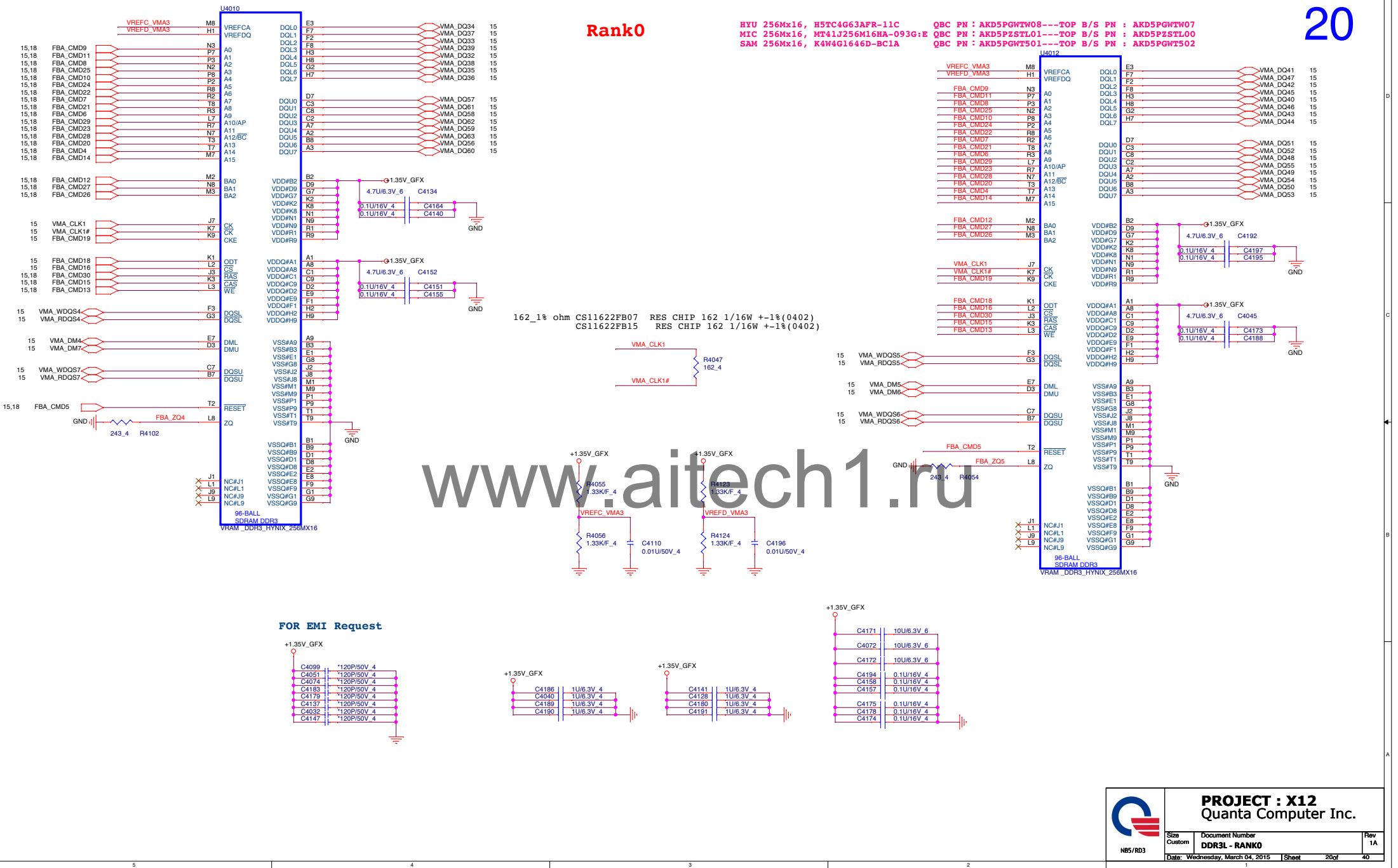
www.aitech1.ru

| | | |
|--|---|-----------|
|  NB5 | PROJECT :Y05 Quanta Computer Inc. | Rev 1A |
| | | |
| Size Custom | Document Number DDR3L - RANK1 | |
| Date: Wednesday, March 04, 2015 Sheet 19 of 40 | | |


Rank0

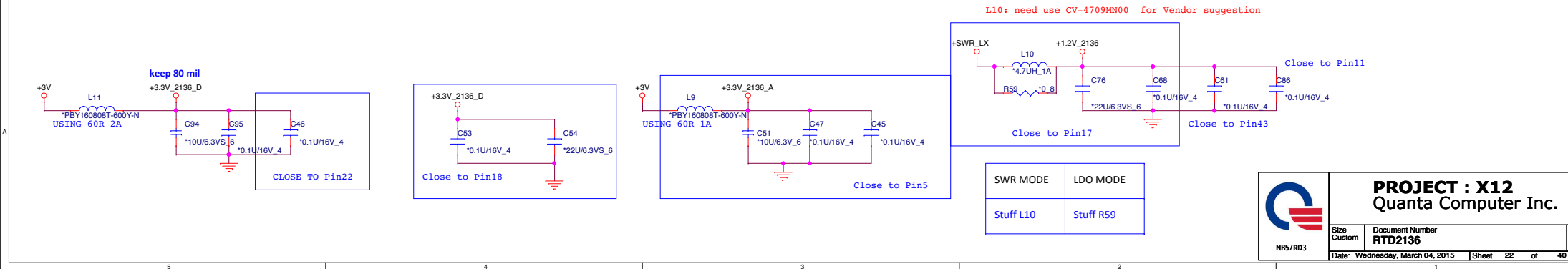
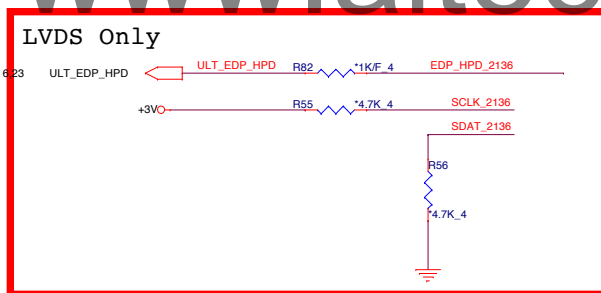
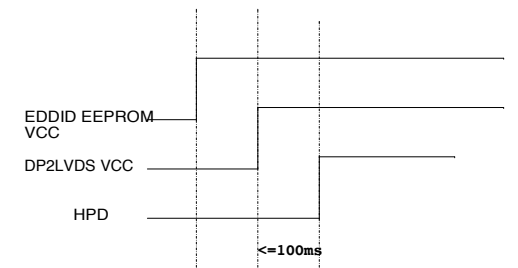
HYU 256Mx16, H5TC4G63AFR-11C
 MIC 256Mx16, MT41J256M16HA-093G:E
 SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
 QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

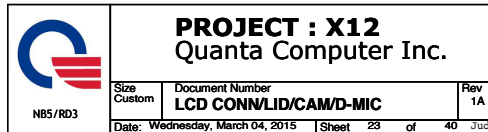
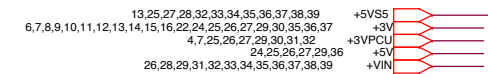
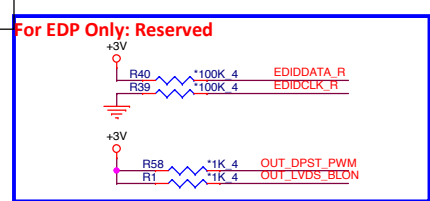
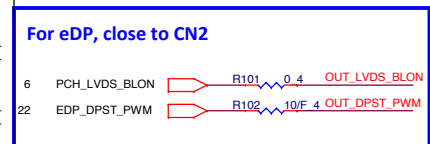
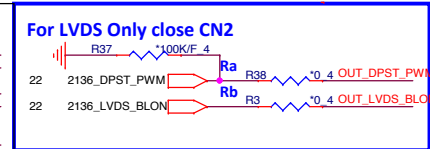
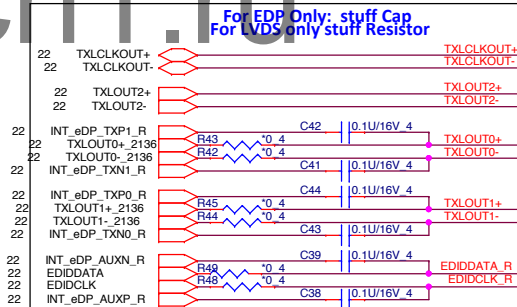
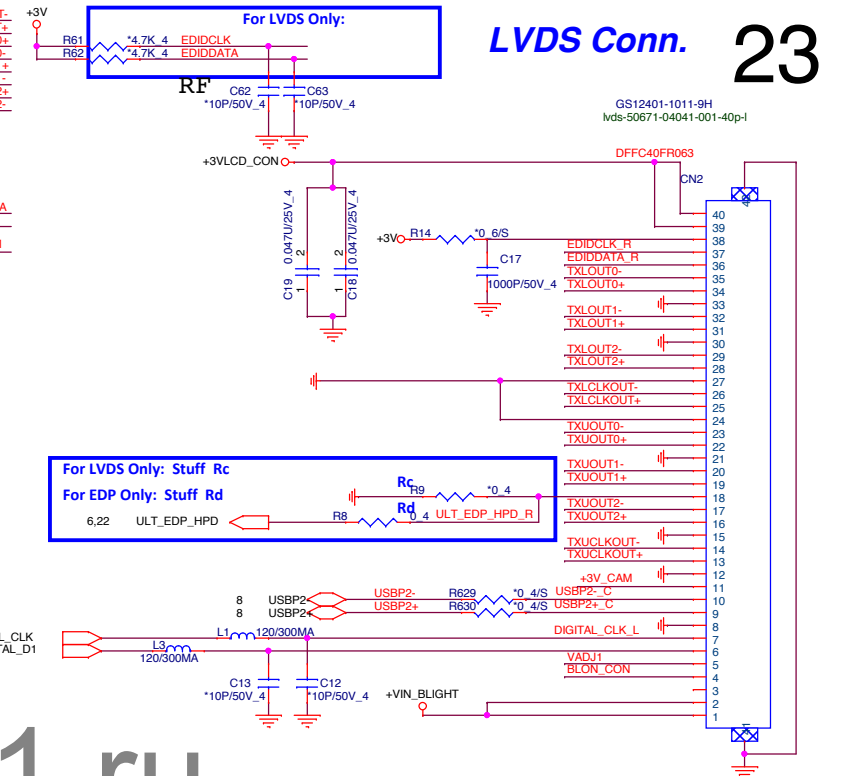
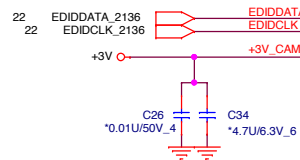
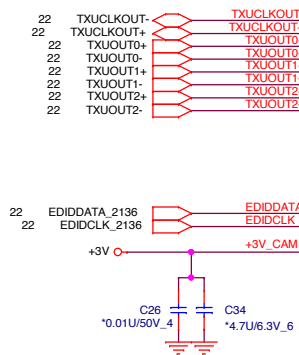
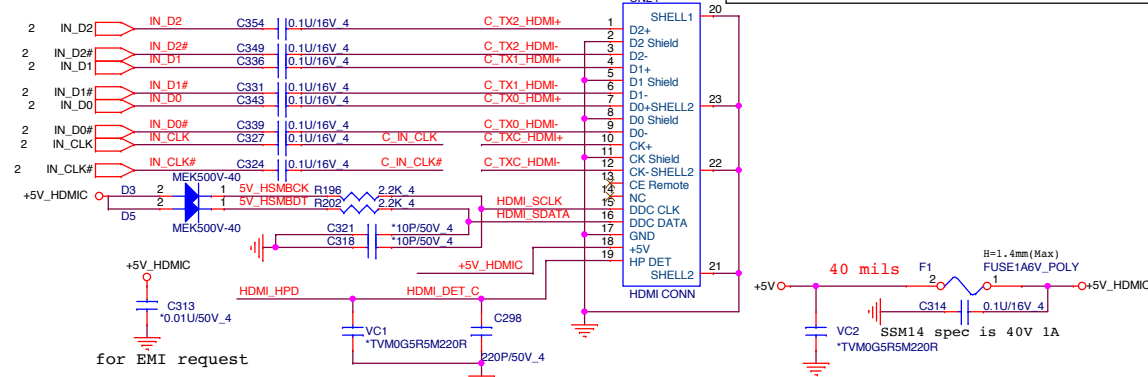
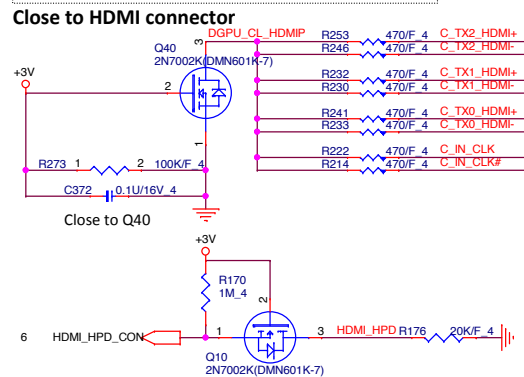
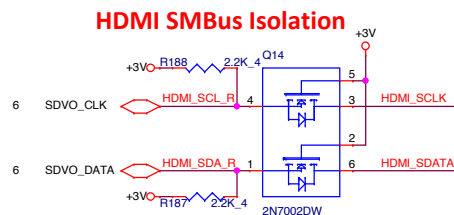
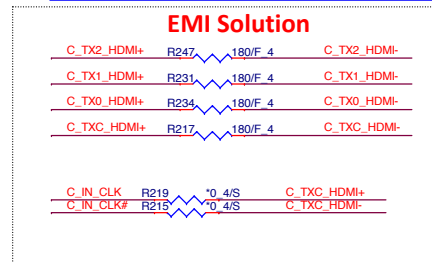
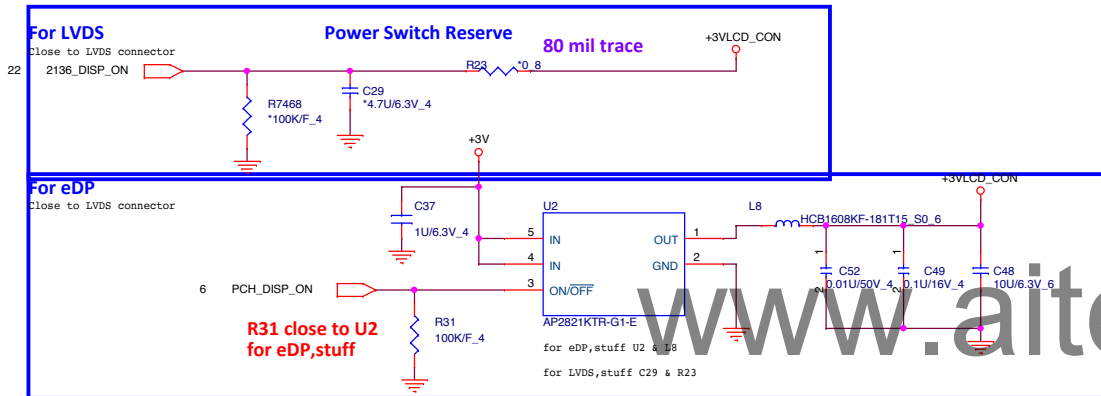
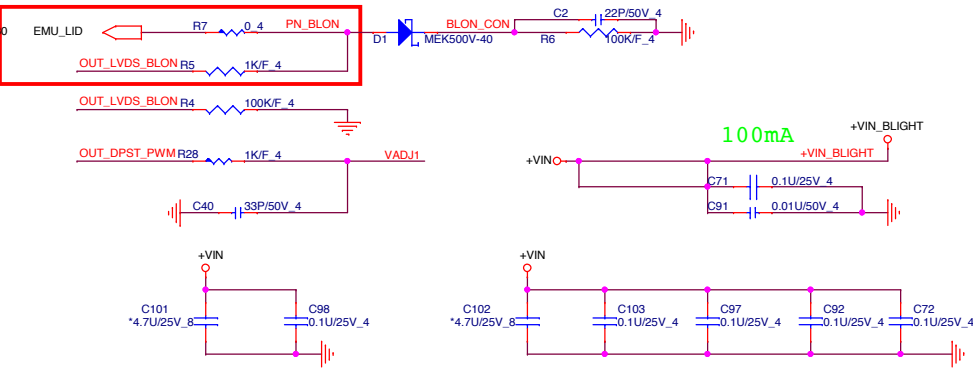


www.aitech1.ru

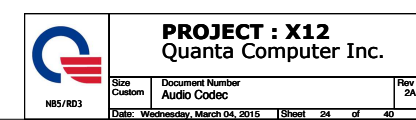
| | | |
|--|---|-----------|
|  NB5 | PROJECT :Y05 Quanta Computer Inc. | Rev 1A |
| | | |
| Size Custom | Document Number DDR3L - RANK1 | |
| Date: Wednesday, March 04, 2015 Sheet 21 of 40 | | |

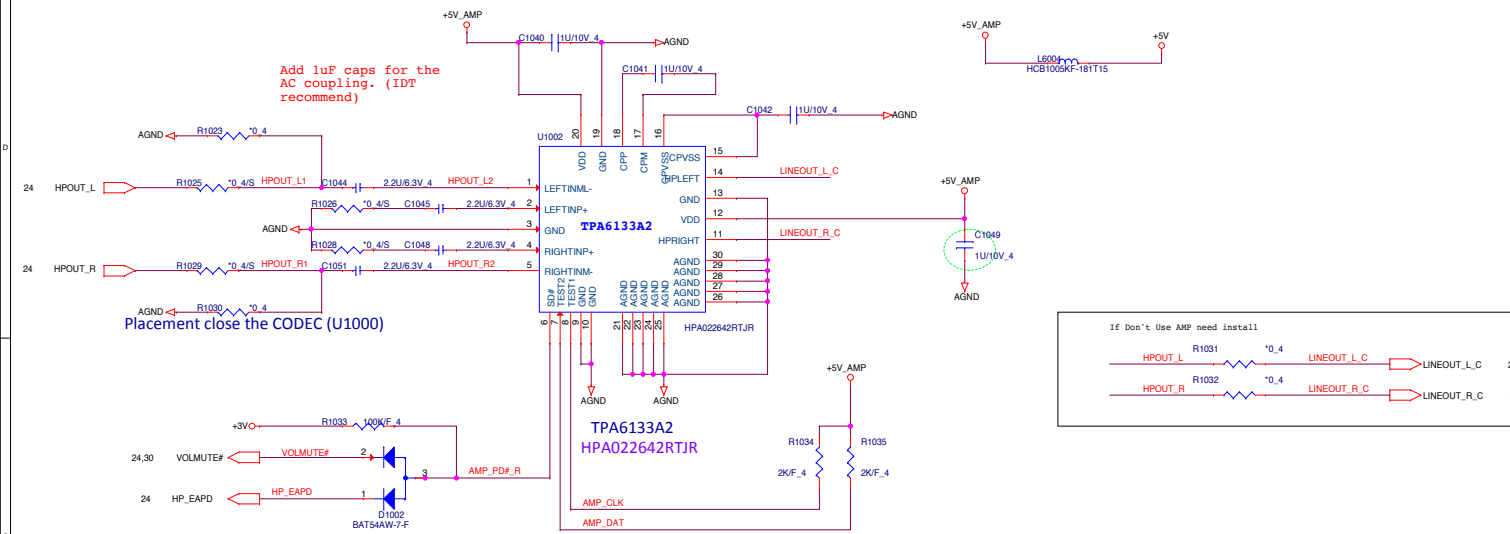


LID Switch

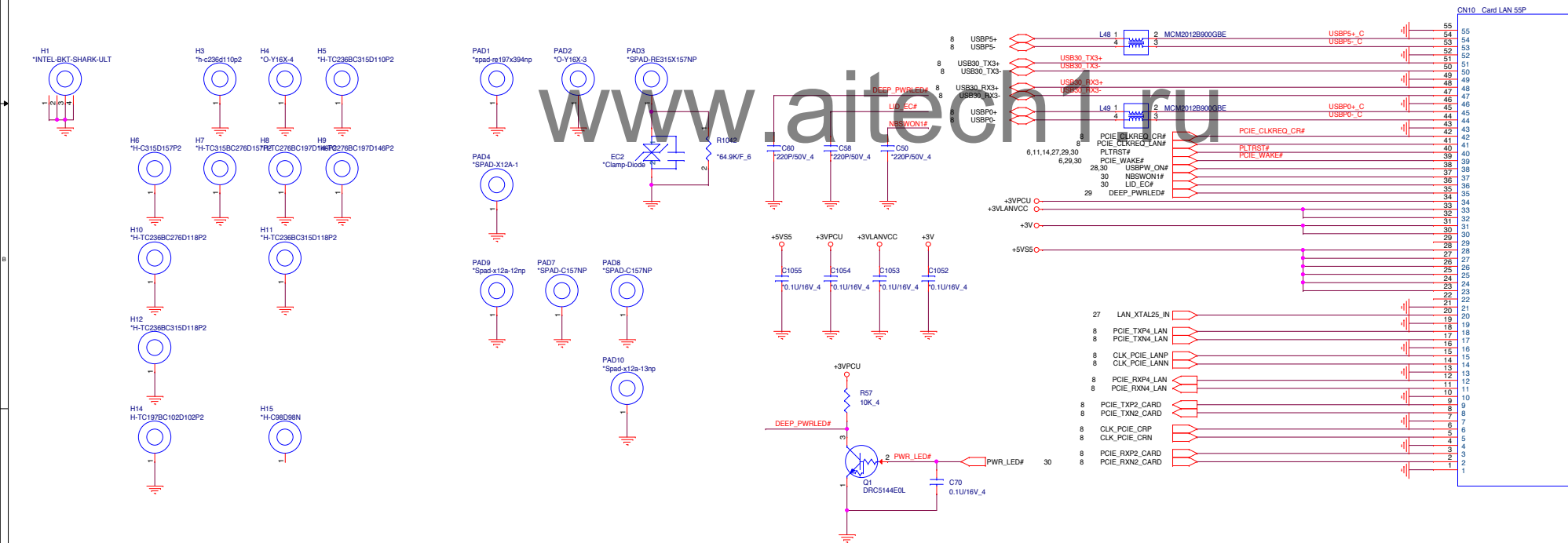


24

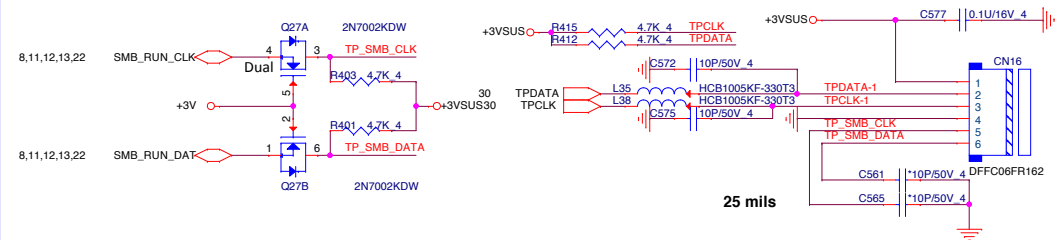




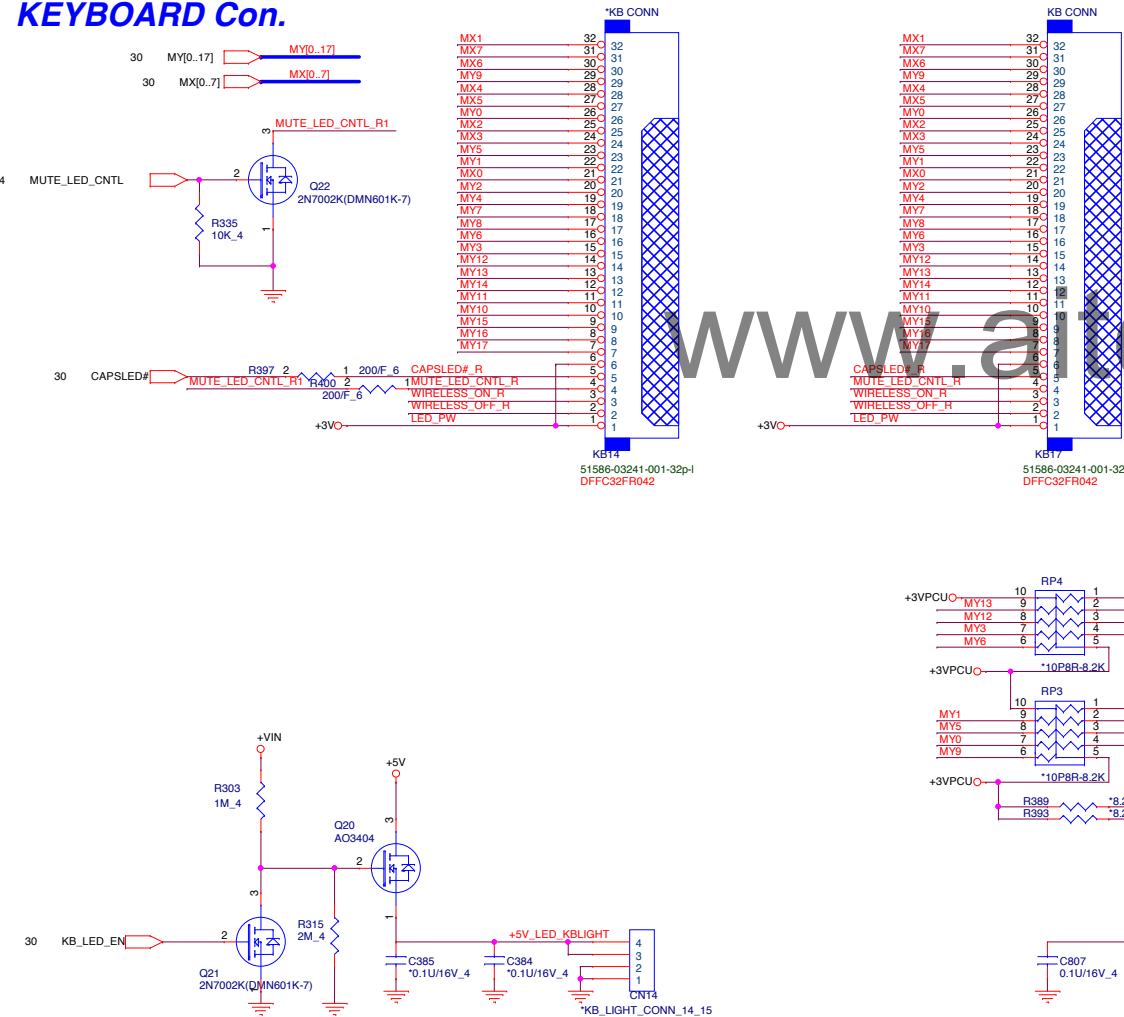
HOLE



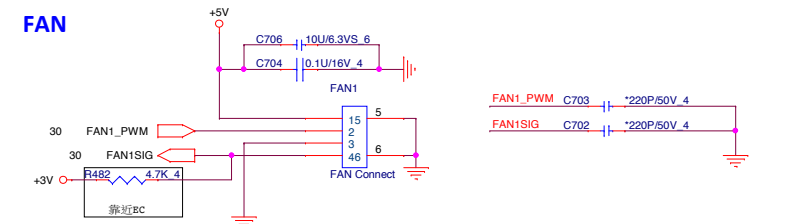
Touch Pad Connector



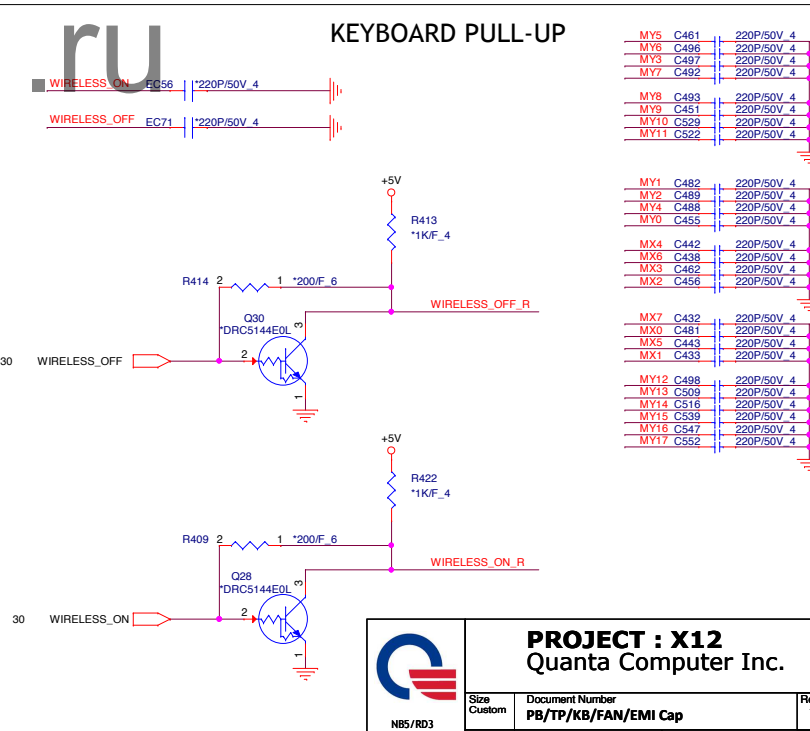
KEYBOARD Con.

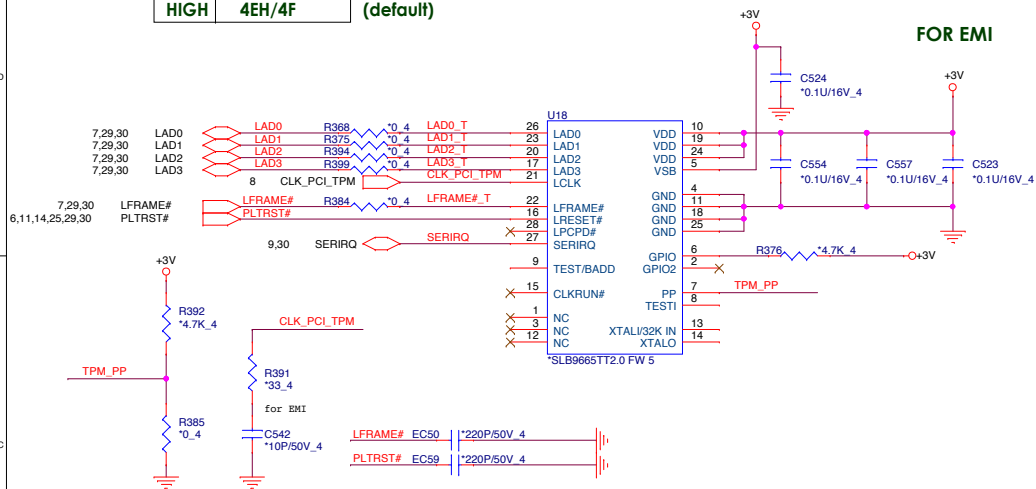


FAN



KEYBOARD PULL-UP

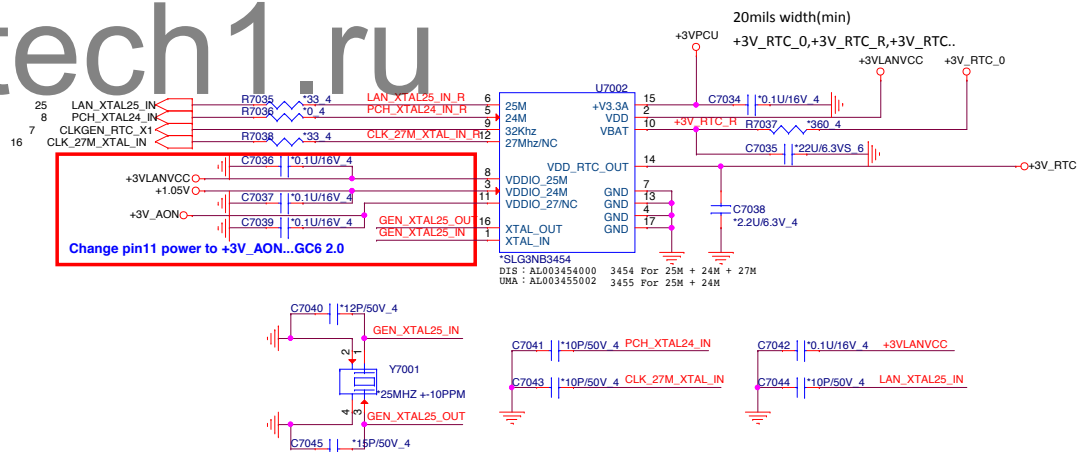




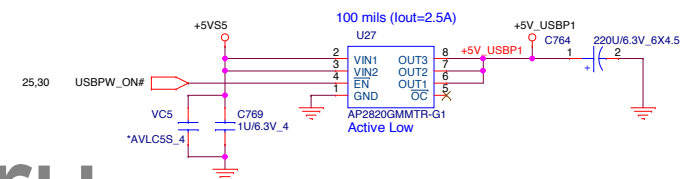
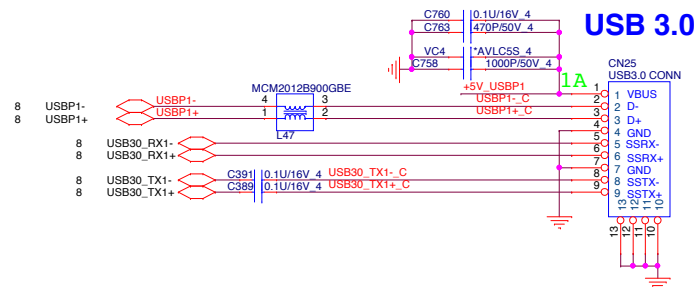
The schematic diagram illustrates the USB-to-TS interface circuit, featuring two identical stages. Each stage consists of a MOSFET driver (Q816, Q817, Q42, Q43) and a USB-to-TS converter (CN4). The circuit is powered by +3V5S, +5V5S, +5V, and +VCC_TS_5V. It includes various resistors (R7466, R7467, R7465, R634, R635, R636) and capacitors (C939, C940, C810, EC3, C21, C778, C779). The output of the converter is TS_ON. A note indicates 'Reserved for ESD 2/24'.

ADD for ON-SELL touch

27



The diagram shows two clamp diode circuits. On the left, a diode labeled EC79 is connected to the USBP7- line. Its cathode is connected to ground through a capacitor. On the right, a diode labeled EC80 is connected to the USBP7+ line. Its cathode is also connected to ground through a capacitor.

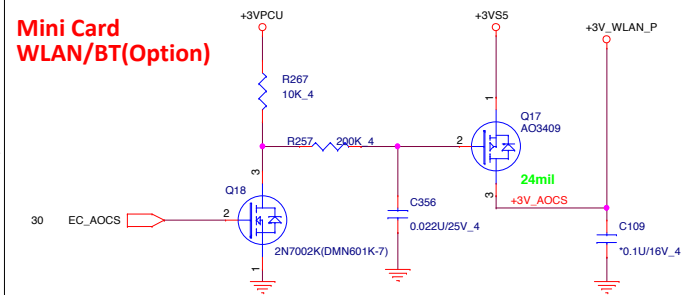


www.aitech1.ru

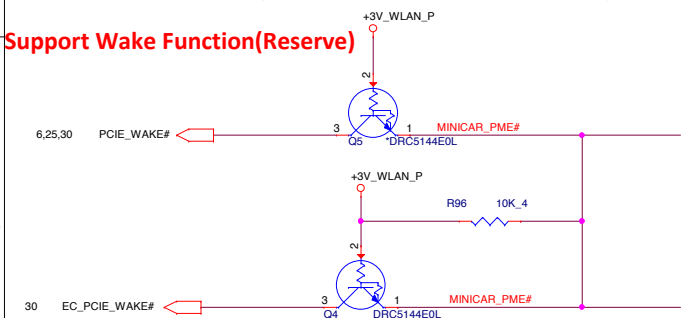
EMI CAP



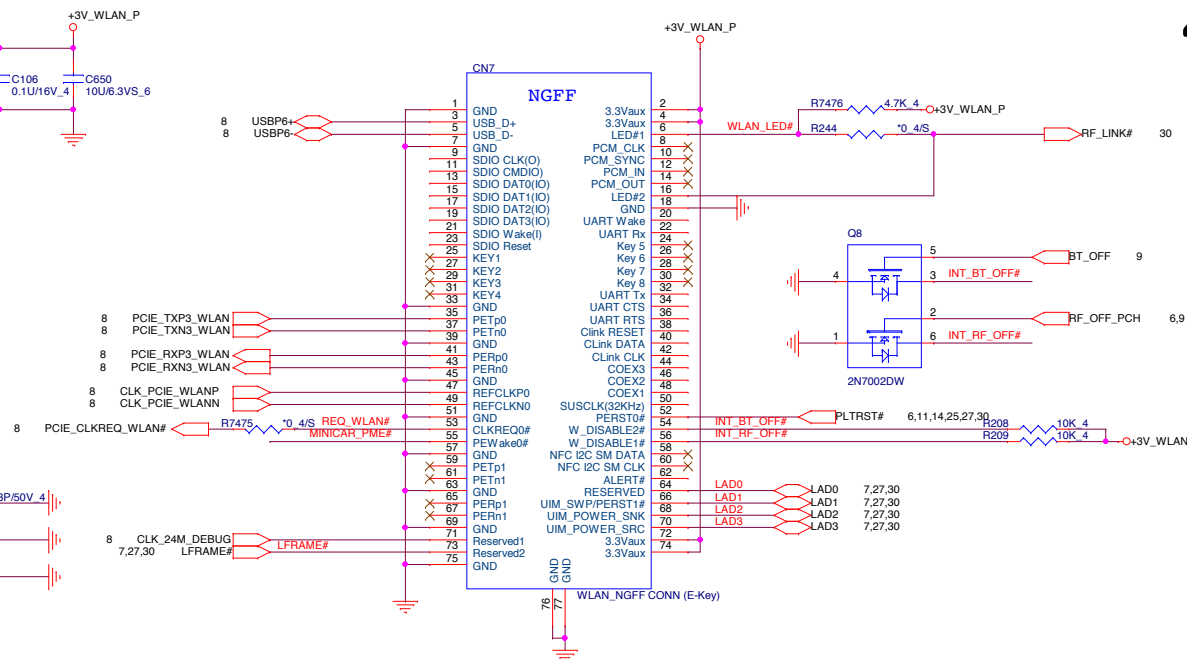
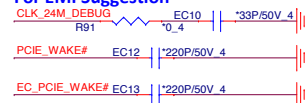
Mini Card WLAN/BT(Optional)



Support Wake Function(Reserve)

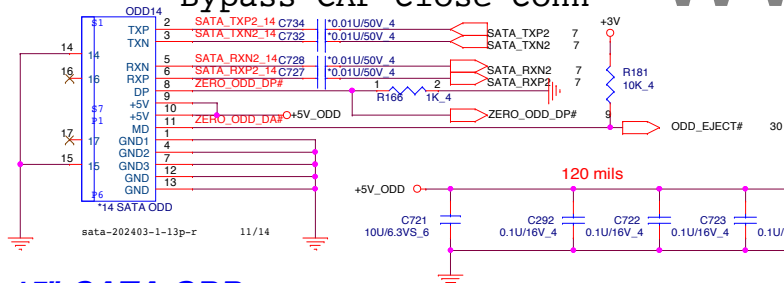


For EMI Suggestion

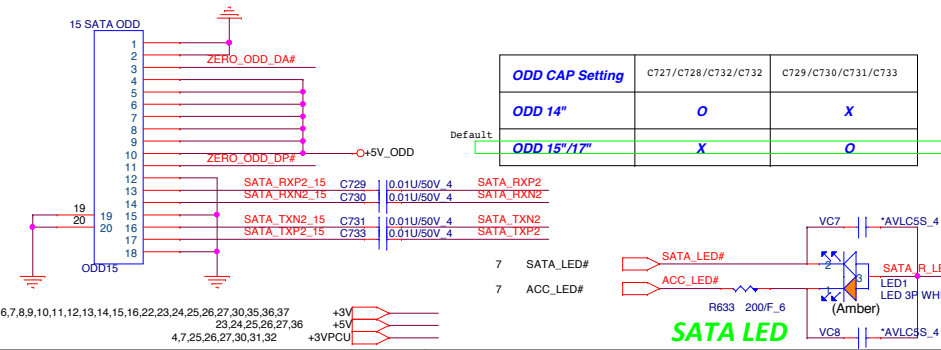


14" SATA ODD

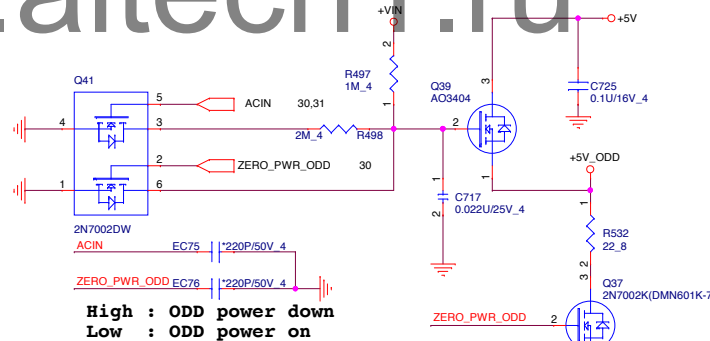
Bypass CAP close conn



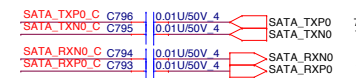
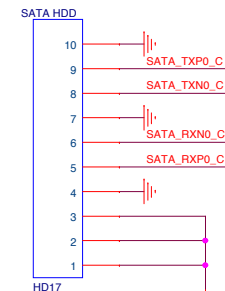
15" SATA ODD



www.aitech1.ru

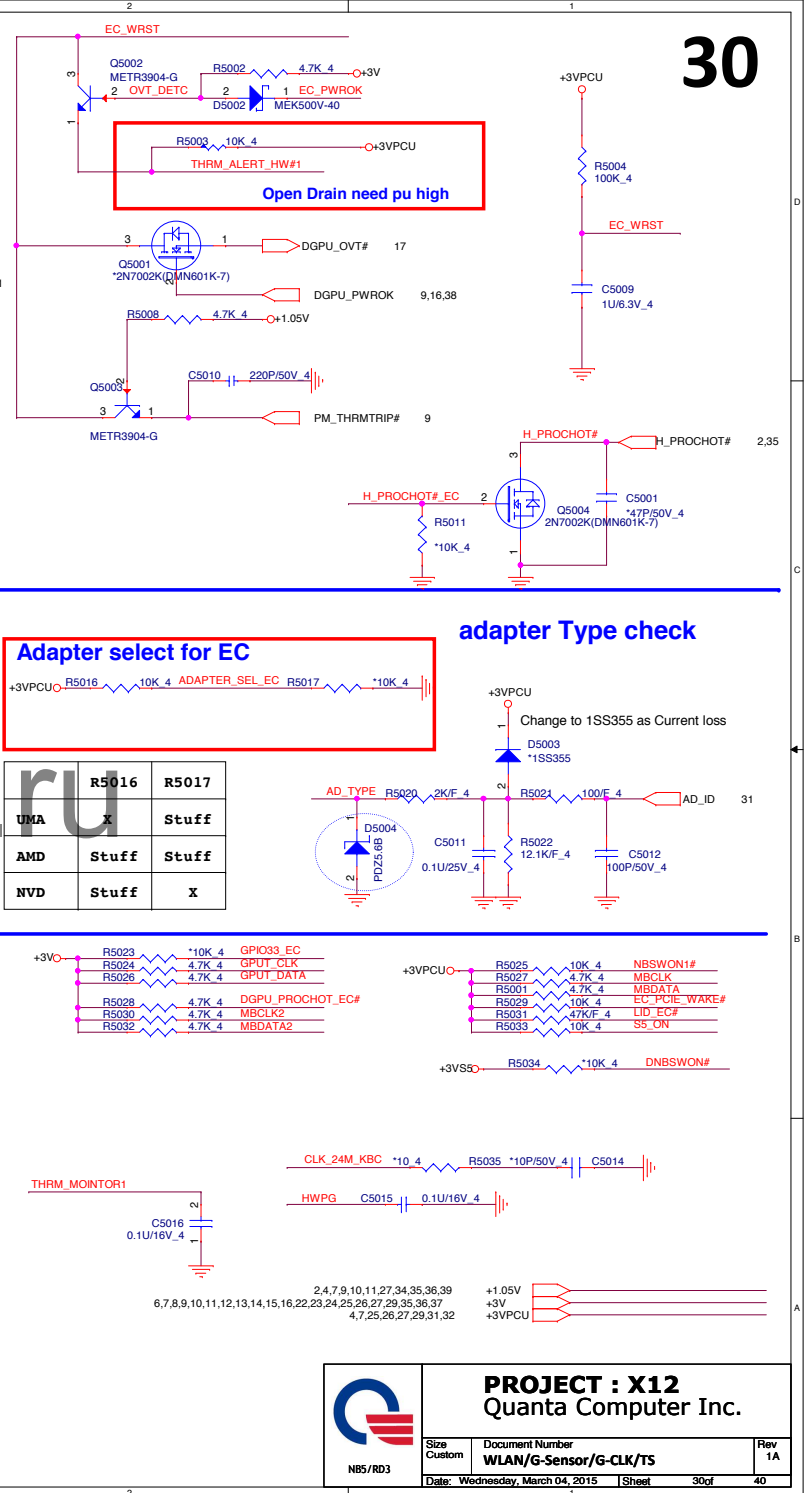


HDD



PROJECT : X12
Quanta Computer Inc.

| Size | Document Number | Rev |
|---------------------------------|-----------------|-----|
| Custom | WLAN/NGFF/MSATA | 1A |
| Date: Wednesday, March 04, 2015 | Sheet 29 of 40 | |

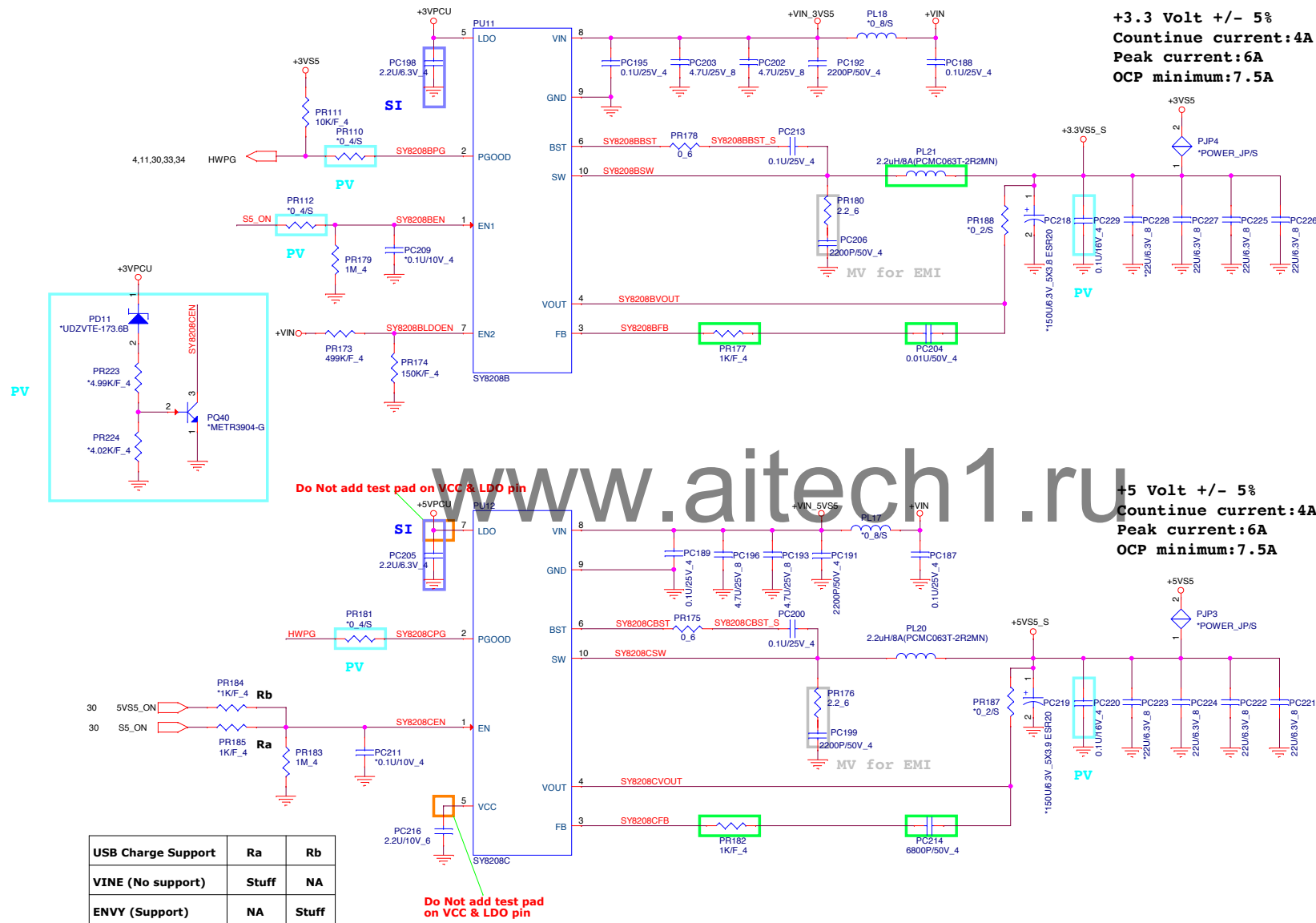




+3VS5 6,9,10,11,27,29,30,34,36,39
+5VS5 13,25,27,28,33,34,35,36,37,38,39

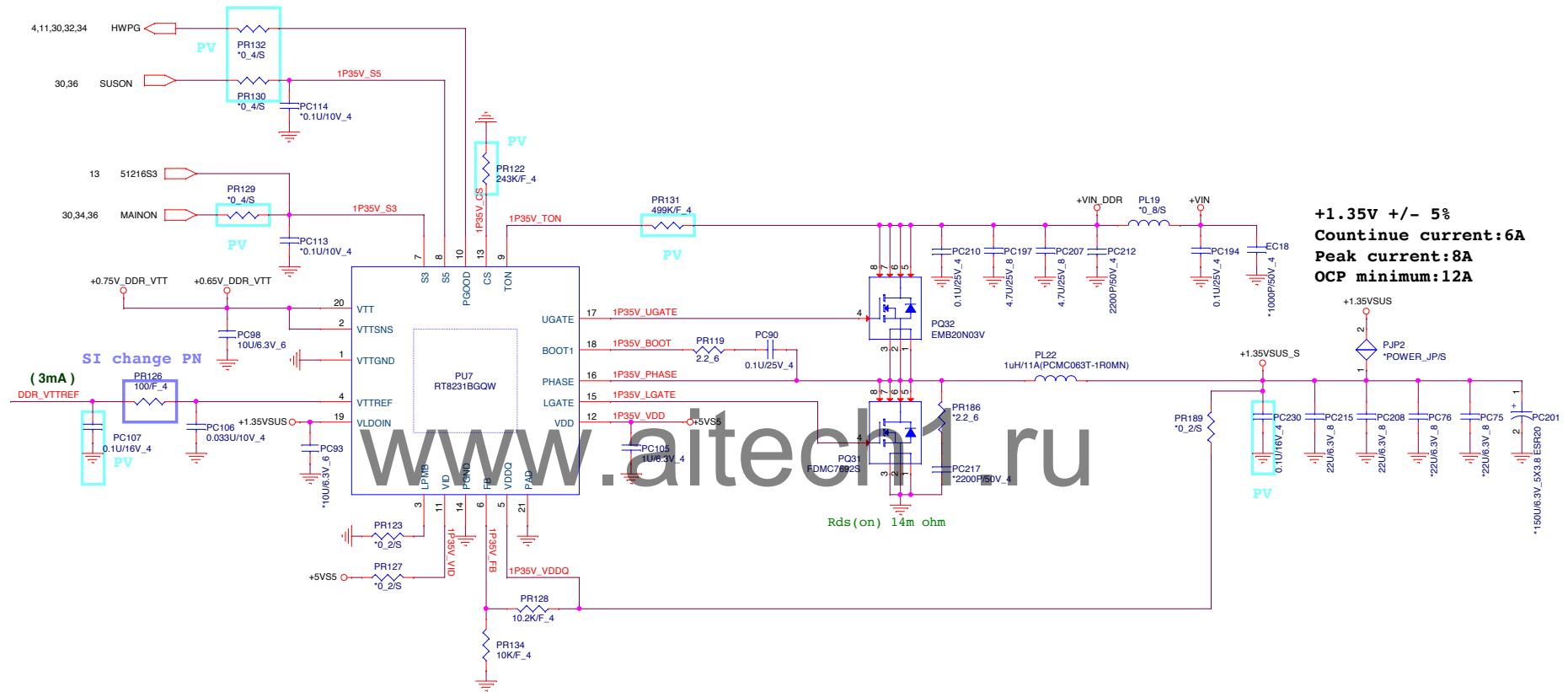
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



PROJECT : X12
Quanta Computer Inc.

Size Custom Document Number **3/5VPCU(RT8243A)** Rev 1A
Date: Wednesday, March 04, 2015 Sheet 32 of 40

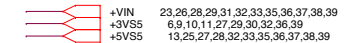


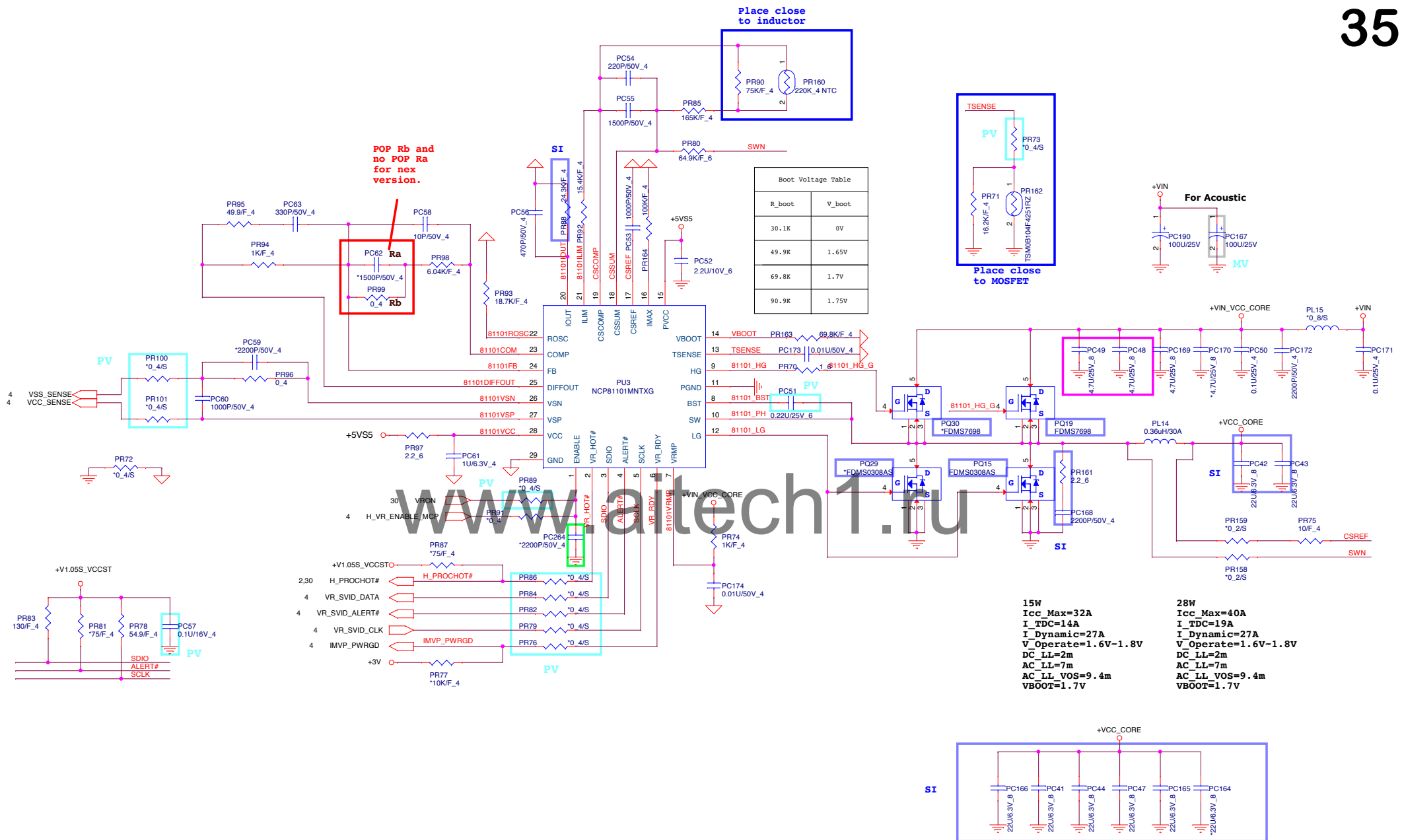
+1.35VSUS 2,4,12,13

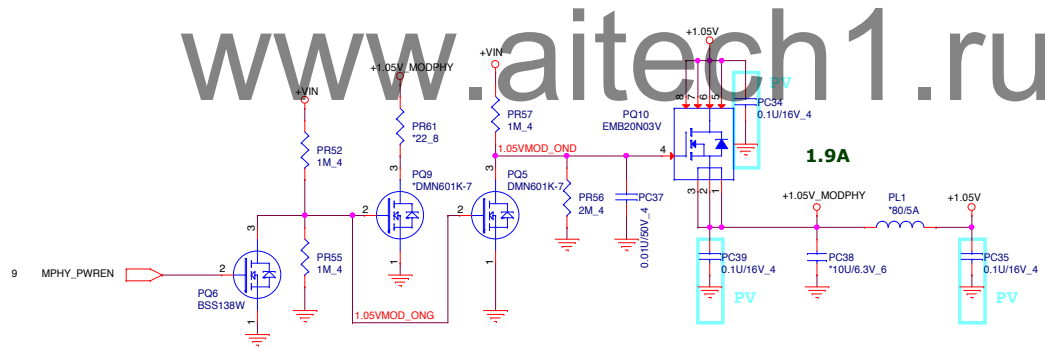
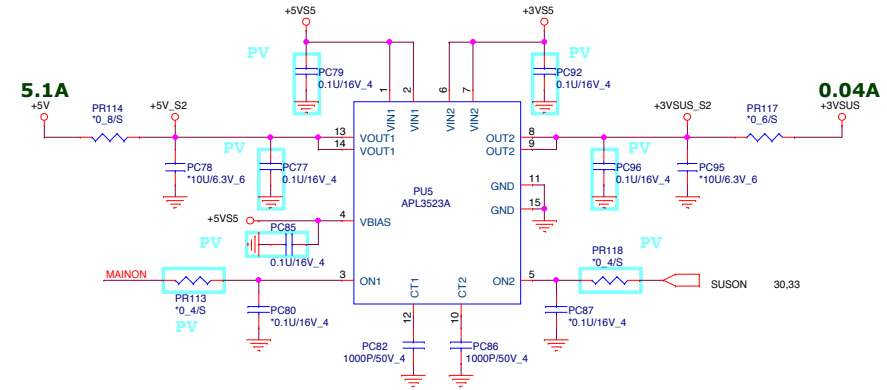
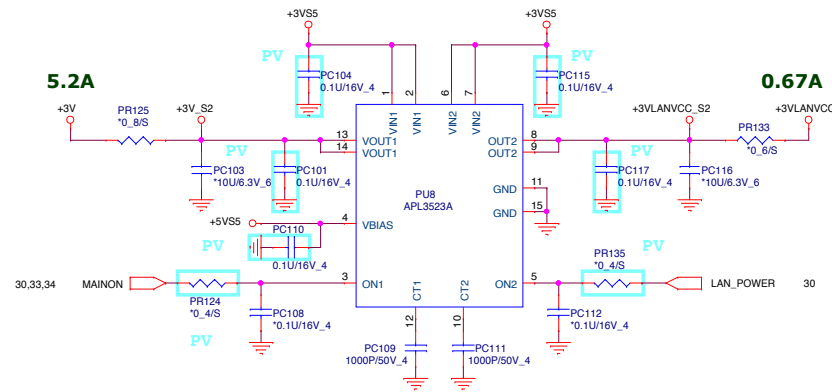


PROJECT : X12
Quanta Computer Inc.

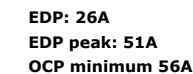
| | | |
|---------------------------------|---|-----------|
| Size Custom | Document Number DDR3 (RT8231A)/1.8VS5 | Rev 1A |
| Date: Wednesday, March 04, 2015 | Sheet 33 | of 40 |

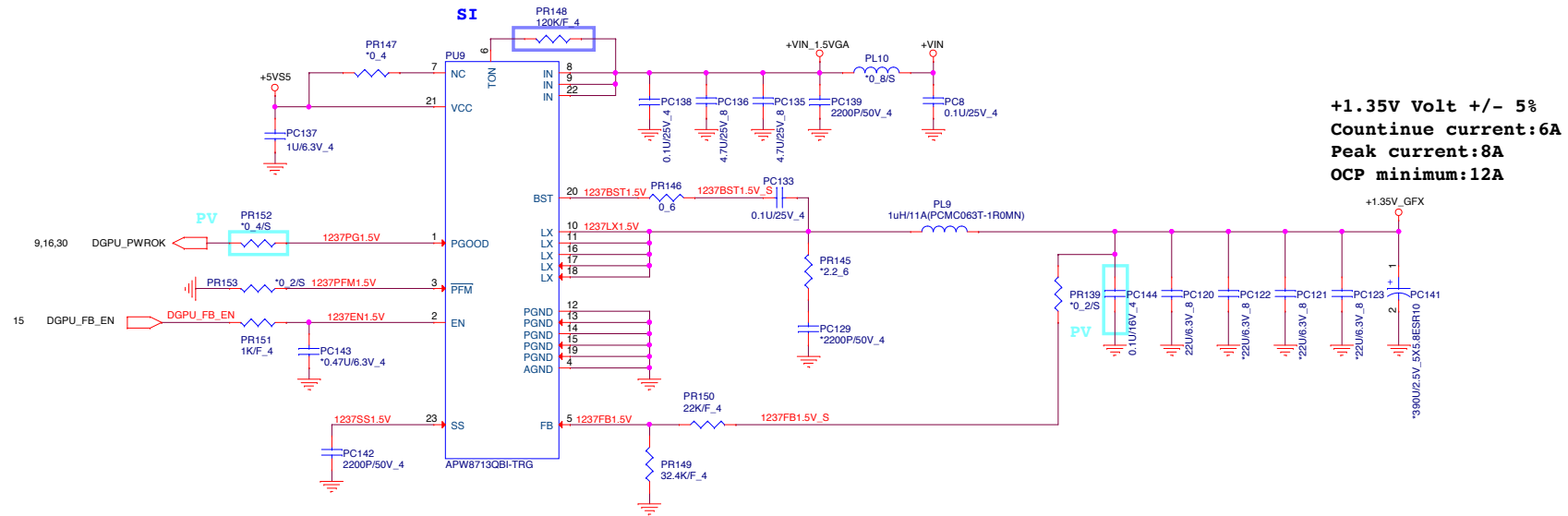




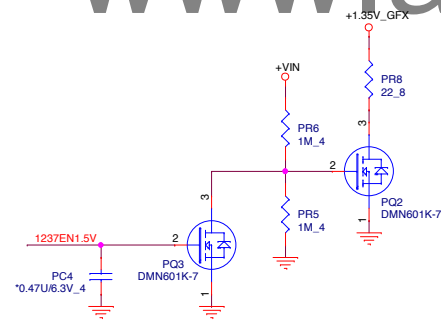


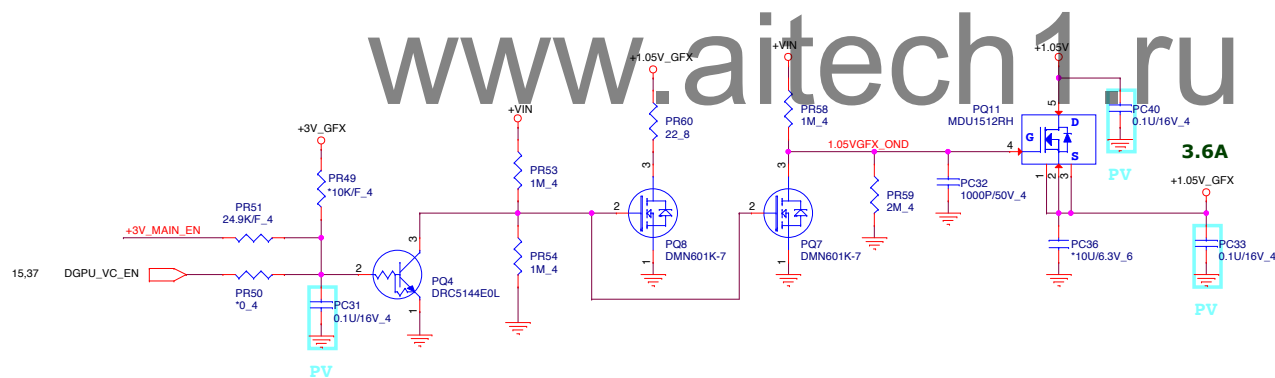
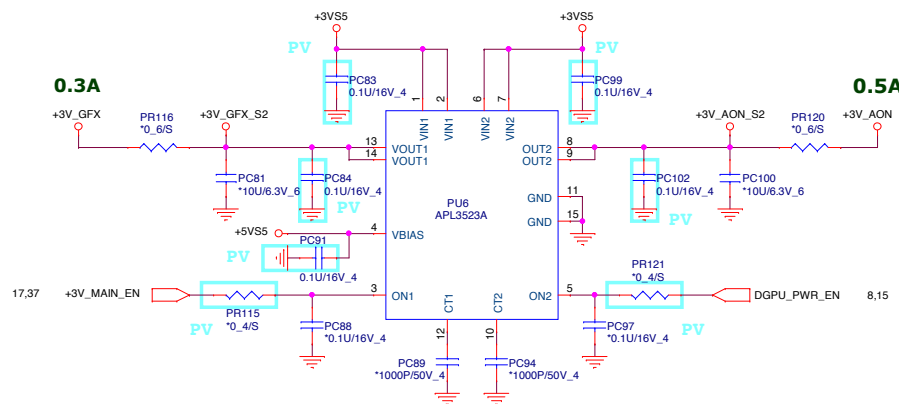
| | |
|--|-----------|
| 6,7,8,9,10,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,37 | +3V |
| 23,24,25,26,27,29 | +5V |
| 23,26,28,29,31,32,33,34,35,37,38,39 | +VIN |
| 6,9,10,11,27,29,30,32,34,39 | +3VS5 |
| 13,25,27,28,32,33,34,35,37,38,39 | +5VS5 |
| 25,27 | +3VLANVCC |





www.aitech1.ru



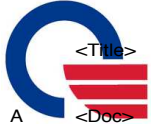


| Battery Connector | Pavillion | ENVY |
|-------------------|-----------|------|
| 14" | - | - |
| 15" | - | - |
| 17" | - | - |

| USB Charge Support | PR185 | PR184 |
|--------------------|-------|-------|
| Pavillion | Stuff | NA |
| ENVY (USB charge) | NA | Stuff |

| UMA | Disable Page 41 、 42 、 43 ,but keep below location |
|---------|--|
| Page 41 | PC161 、 PC162 |
| Page 42 | PC138 、 PC144 、 PC4 、 PC148 |
| Page 43 | PC84 、 PC102 、 PC88 、 PC97 、 PC40 、 PC33 |

| Discrete | Location | Part Number |
|------------|---------------------------|-------------|
| N15S (25W) | PR155 | CS29532FB10 |
| | PC151 、 PC160 | NA |
| | PQ21 、 PQ23 、 PQ25 、 PQ28 | NA |
| N15P (35W) | PR155 | CS31242FB13 |
| | PC151 、 PC160 | Stuff |
| | PQ21 、 PQ23 、 PQ25 、 PQ28 | Stuff |

| | | | |
|---|---------------------------|-----------------|-----|
|  | PROJECT : X12 | | |
| | Quanta Computer Inc. | | |
| | Size | Document Number | Rev |
| NB5/RD3 | Wednesday, March 04, 2015 | 40 | 40 |
| Date: | Sheet of | | |